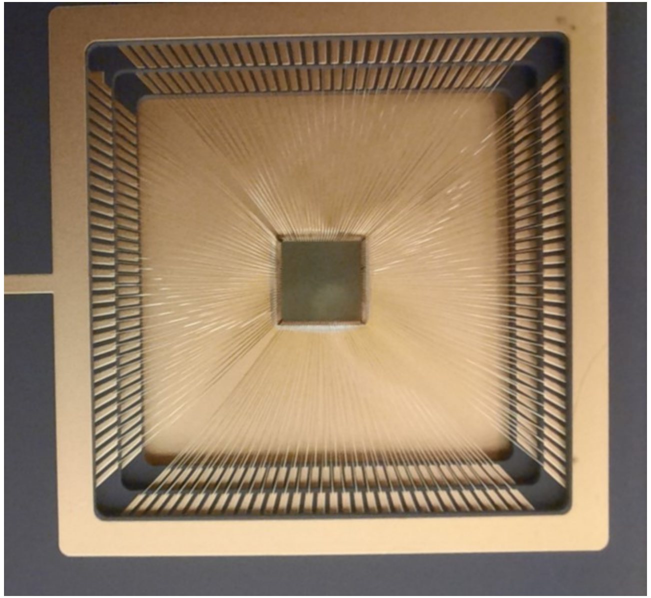
Tampereen yliopisto
Tampere University

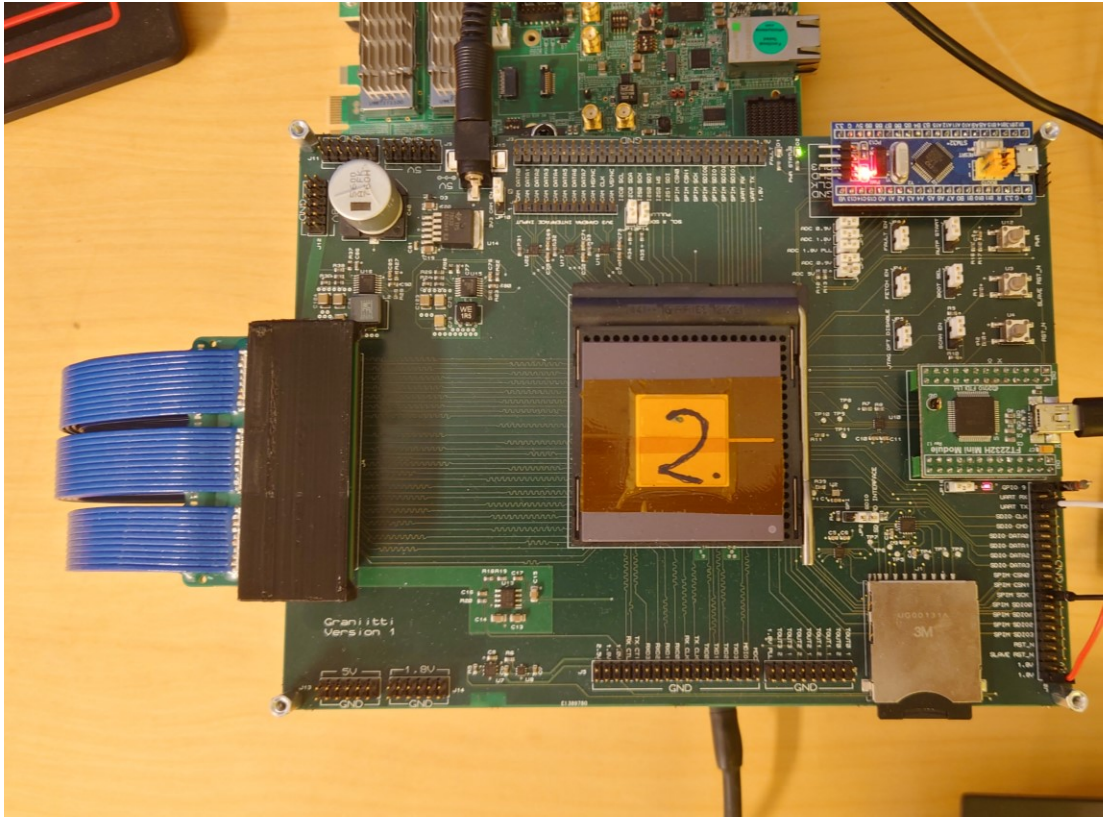
COMP.CE.250
System-on-Chip Design

System-on-Chip?

Arto Oinonen

System-on-Chip Ballast





What does "System" mean here?

System-on-Chip

- *"Integrates all the components of a computer into a single piece of silicon"*

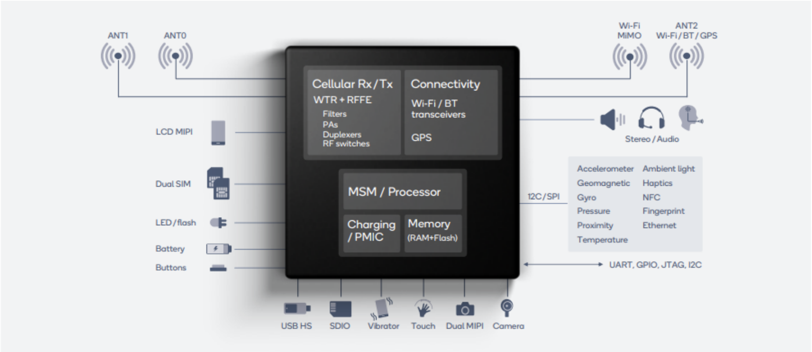
- Computer:
  - CPU
  - Internal peripherals
  - Interfaces
    - Memory
    - Storage
    - I/O
    - Radios
  - Accelerators
  - Shared memories
  - DMAs
  - …

Qualcomm® Snapdragon™

System-in-Package

Qualcomm snapdragon

SPECIFICATIONS & FEATURES



Modem
- Snapdragon X9 LTE modem
- Cat 7 downlink, up to 300 Mbps, 2xCA
- Cat 13 uplink, up to 150 Mbps
- 64-QAM UL
- Qualcomm® Snapdragon™ All Mode
- Qualcomm® Snapdragon™ Upload +

Connectivity
- Integrated 802.11ac Multi-User MIMO (MU-MIMO)
- Qualcomm® Location technology Gen8C Lite
- USB version 3.0
- Bluetooth version 4.2 + BLE

CPU
- 8x Arm Cortex A53
- Up to 1.8 GHz
- 14nm process technology

DSP

Qualcomm® Hexagon™ 546 DSP

GPU
- Qualcomm® Adreno™ 506 GPU
- OpenGL ES 3.1, OpenCL 2.0 Full

Display
- Primary Full HD+
- One 4-lane DSI
- Qualcomm® Low-Power Picture Enhancement support
- Qualcomm® TruPalette™ Display Feature support
- Qualcomm® improveTouch™ technology support

Camera
- Support up to 4 cameras
- Three 4-lane CSI at 2.1 Gbps per lane
- Dual concurrent camera operation
- Dual 14-bit image signal processing (ISP):
  - Dual camera: up to 13 MP + 13 MP at 30 fps ZSL
  - Single camera: up to 21 MP at 30 fps ZSL or
  - Single camera: up to 24 MP at 24 fps

Video

FHD+ @ 60 fps HEVC capture & playback

Audio
- Qualcomm Aqstic™ Audio codec (WCD9335)
  - Hi-Fi music playback: 192 kHz/24-bit,
  - Total Harmonic Distortion + Noise (THD+N), Playback: –109 dB
  - Dual Oscillator Support, Playback: 44.1 kHz, 48 kHz
- Qualcomm Aqstic smart speaker amp (WSA881x)
  - Total Harmonic Distortion + Noise (THD+N), Playback: –80 dB
  - Amplifier output power: Up to 4 W
  - Smart speaker protection
- Crystal clear VoLTE w/ Ultra HD Voice (EVS)
- Dolby Digital Plus 5.1 & DTS-HD surround sound
- Qualcomm® Audio & Voice optimization technology

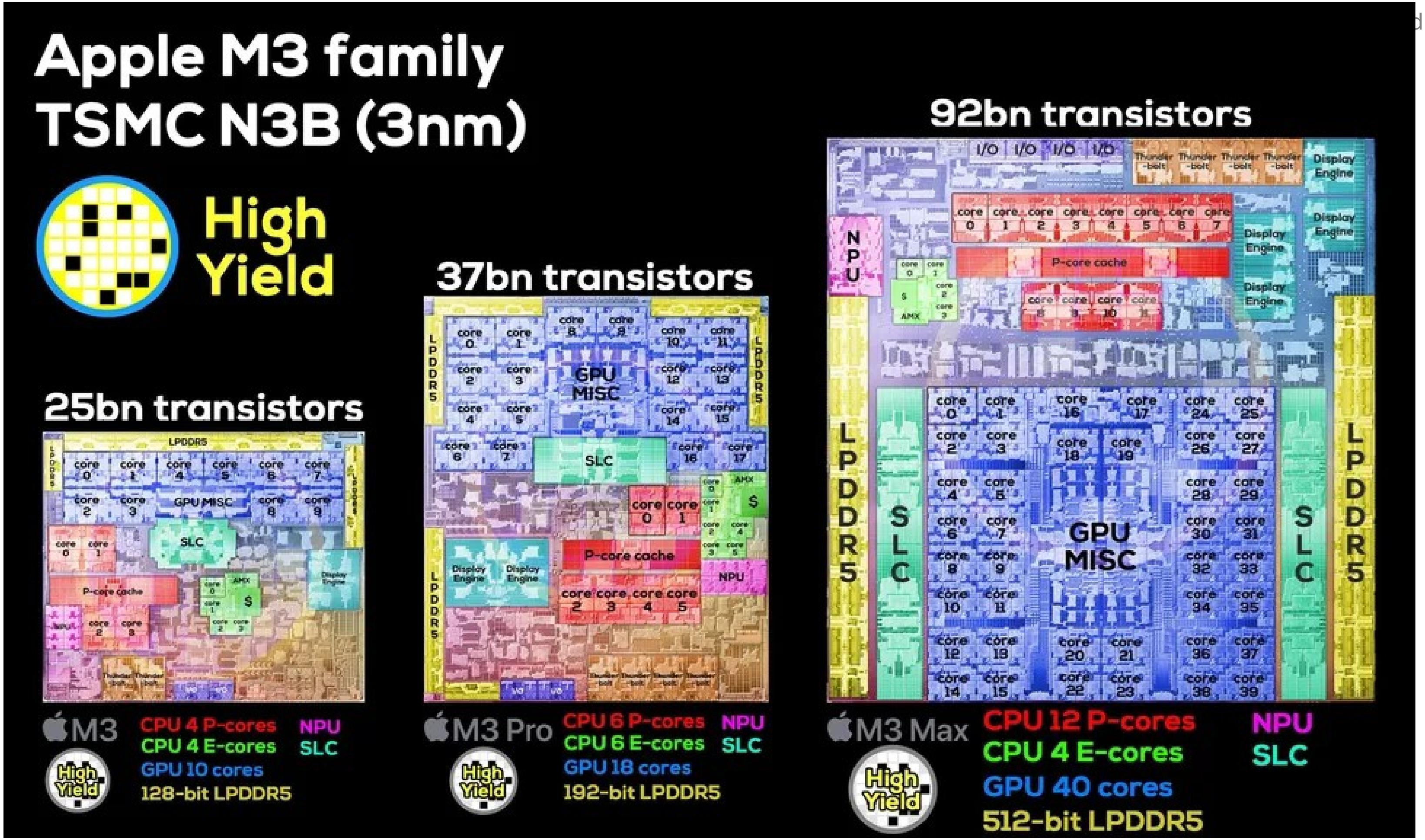
RF Front-End
- Integrated RF Transceiver
- Integrated low-/mid-/high-band Power Amplifier modules
- Integrated Average Power Tracker
- Integrated Dynamic Antenna Tuning solution for superior power efficiency
- Integrated Diversity Antenna Switch

Charging

Qualcomm® Quick Charge™ 3.0 technology

Memory
- eMCP (SDRAM+eMMC), LPDDR3
- Memory Configurations
  - 8 GB RAM + 32 GB ROM
  - 4 GB RAM + 64 GB ROM

https://www.qualcomm.com/products/mobile/snapdragon/smartphones/snapdragon-system-package

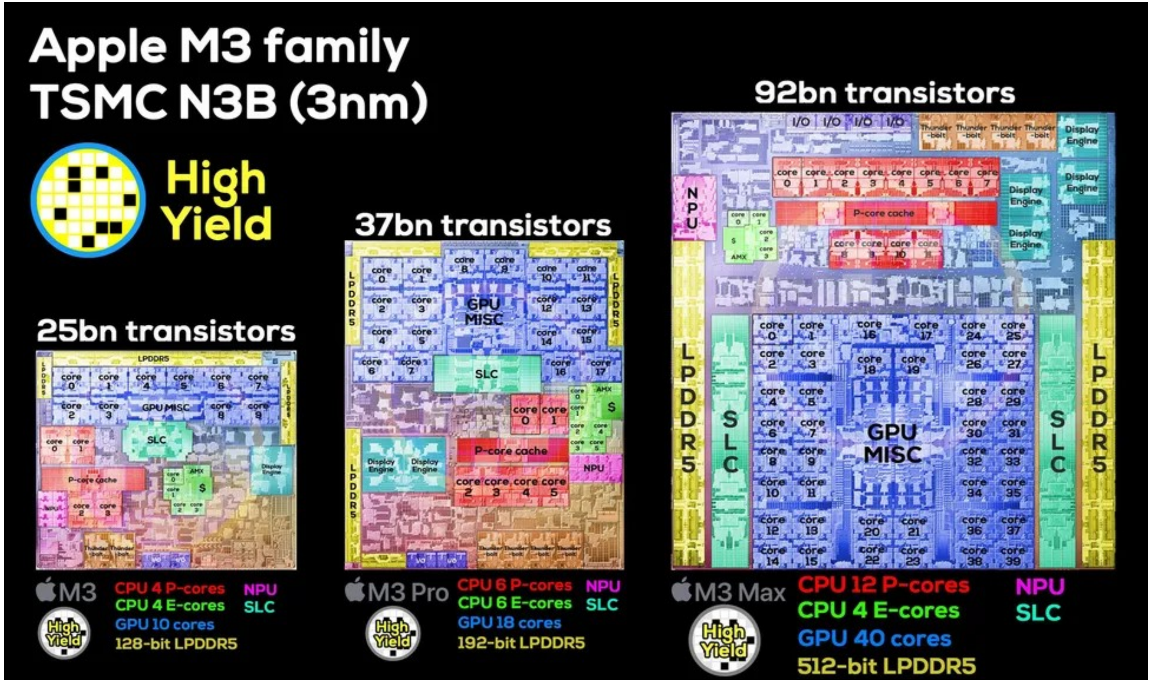


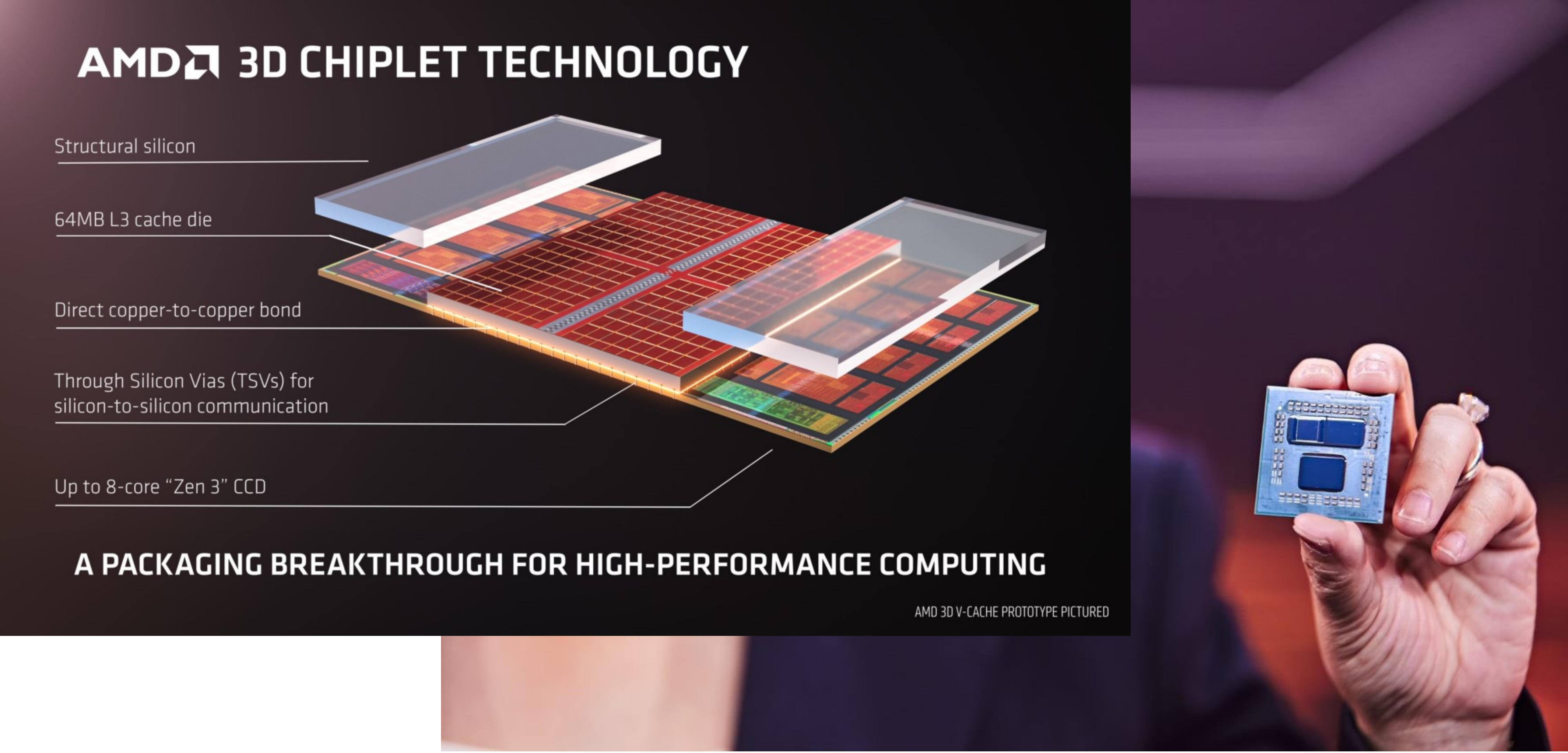
Tampereen yliopisto
Tampere University

Find the differences between these

Cost of scaling

- *”Same internals, more of everything” – more than copy-pasting*
- Area:
  - Price
  - Yield
  - Packaging (Pins)
- Interconnect:
  - Increased area
  - Complexity
  - Arbitration, bottlenecks
- Power:
  - Switching power
  - Leakage current
  - Power delivery
  - Heat transport



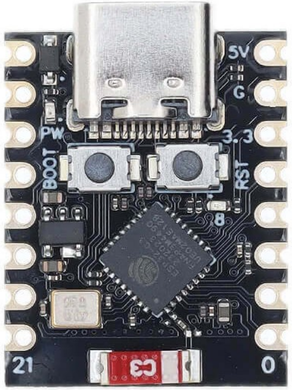


Is this a System-on-Chip?

Tampereen yliopisto
Tampere University

[source https://wccftech.com/amd-confirms-zen-3-ryzen-cpus-with-3d-v-cache-stack-chiplet-design-coming-early-next-year-before-zen-4/]

SoC vs CPU/microcontroller



- Microcontroller: a lightweight SoC, typically:
  - Interfaces useful for sensors, ADC/DAC
  - Integrated memories (volatile & non-volatile)
  - ➢ Low power, cost-effective for simple applications

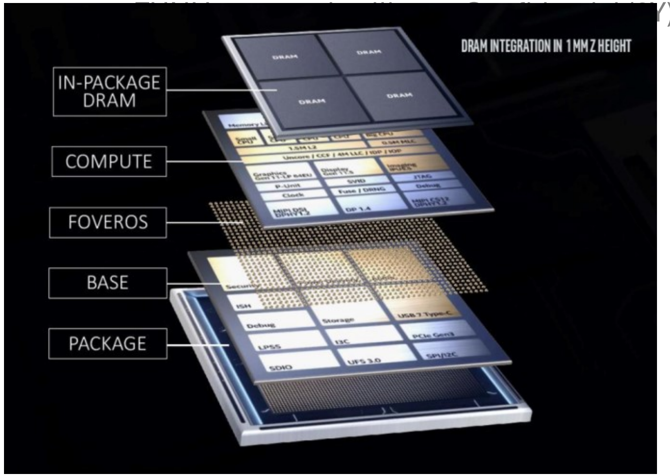
- CPU: Not self-contained
  - Requires additional chips (chipset, memories)
  - ➢ Performance-oriented design

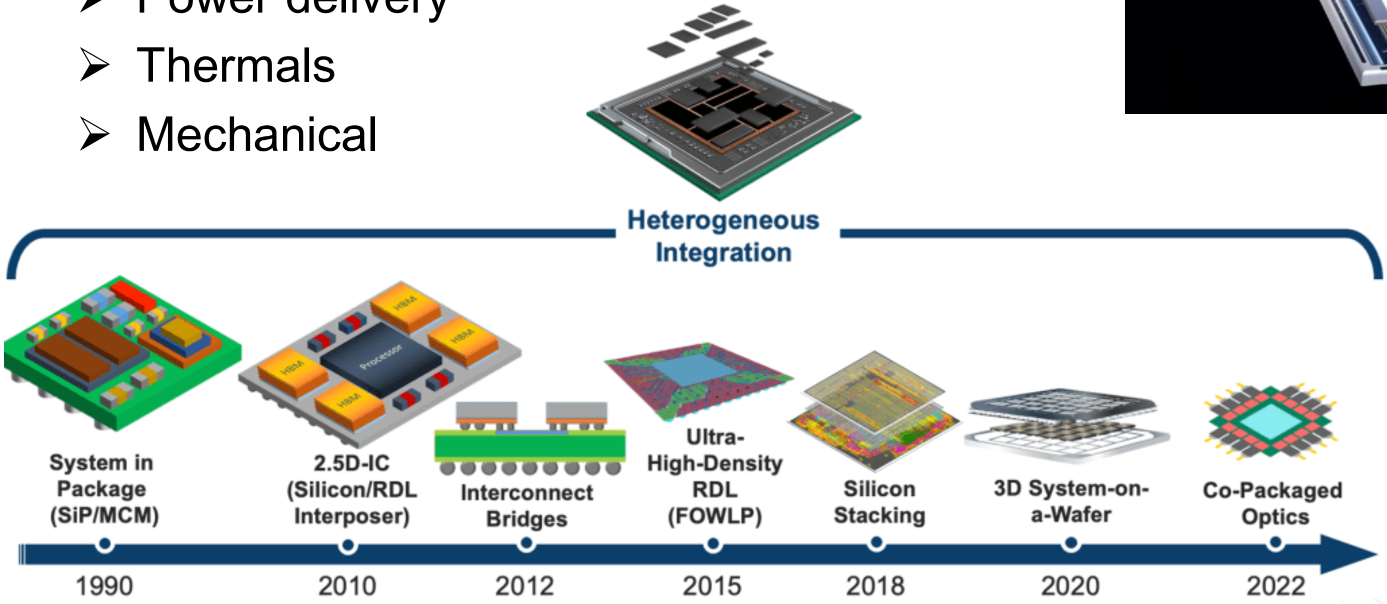
- ALL: Produced in an ASIC process

➢ Focus on different challenges, but same design tools

3d integration

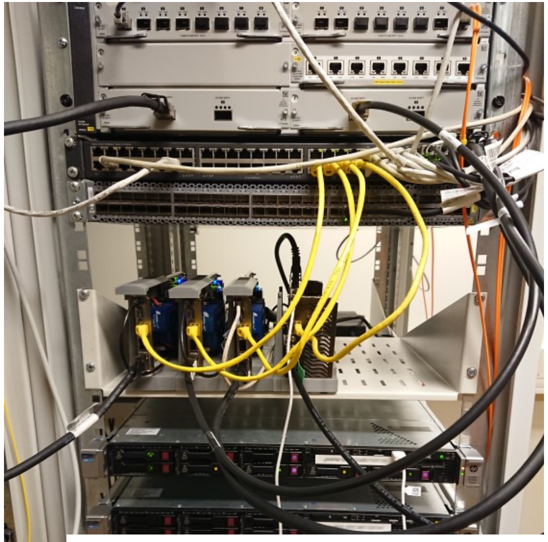
- Old challenges on a new level
  - ➢ C2C interconnects
  - ➢ Power delivery
  - ➢ Thermals
  - ➢ Mechanical

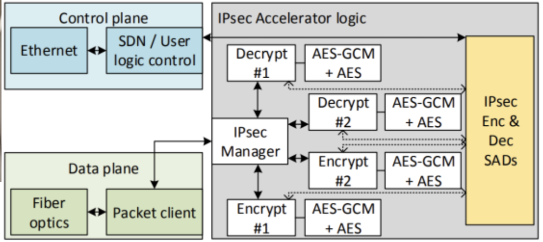




https://semiengineering.com/mechanical-challenges-increase-with-chiplet-integration/
https://www.tomshardware.com/news/intel-lakefield-foveros-3d-chip-stack-hybrid-processor,40205.html

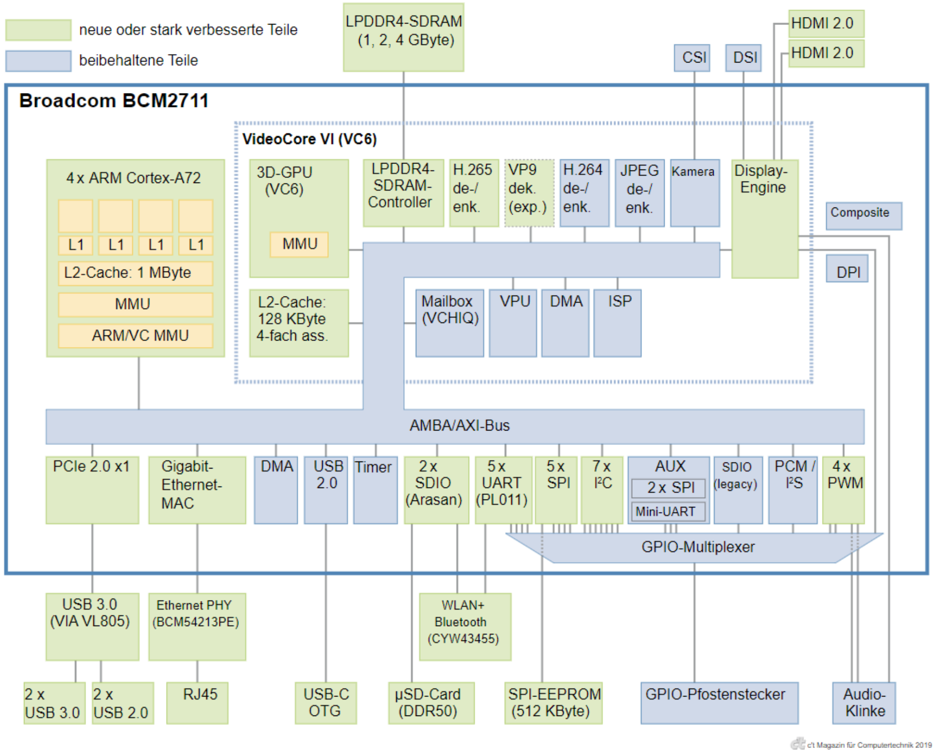
TAU FPGA-accelerated cloud: IPsec accelerator





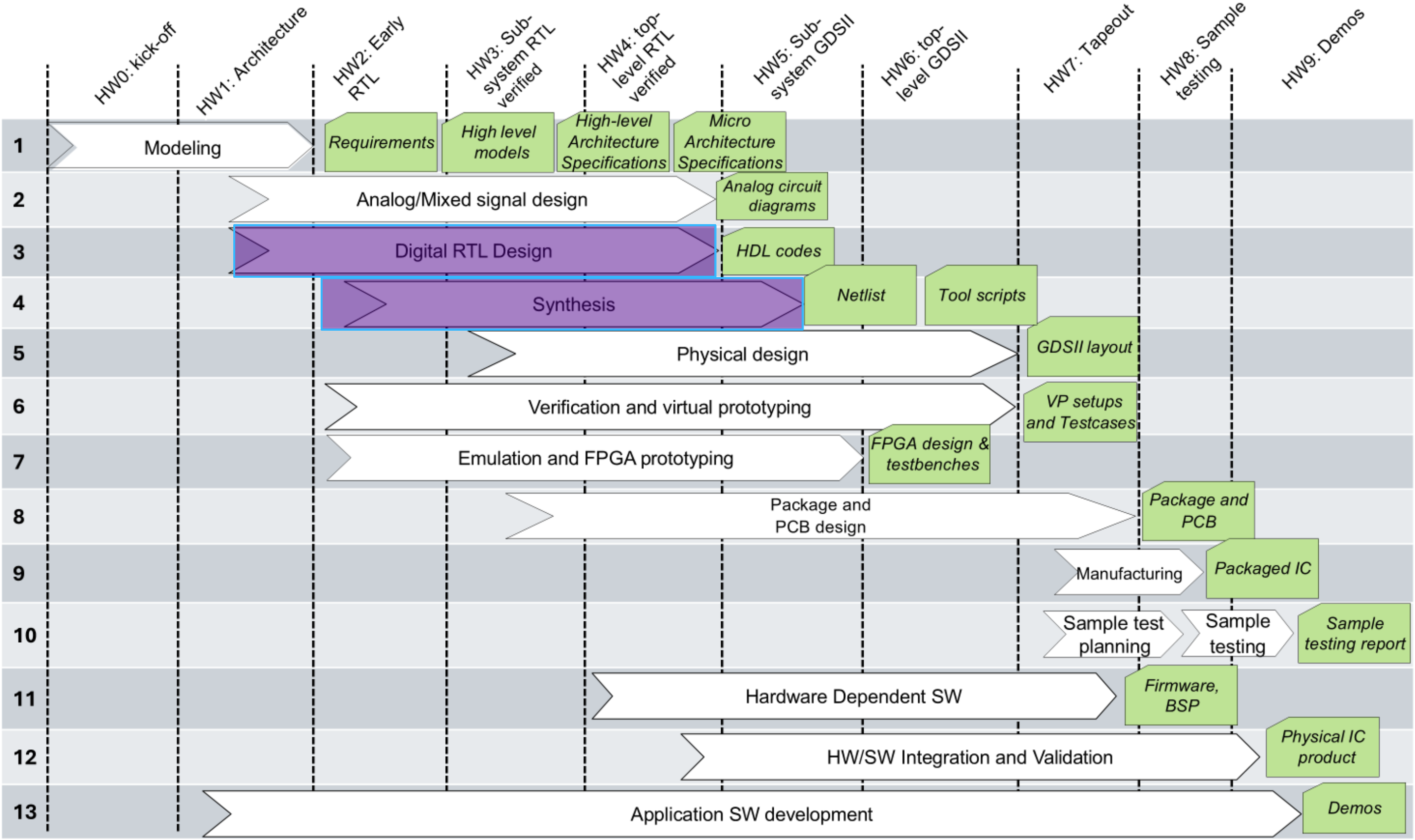
Herz des Raspberry Pi 4: Broadcom BCM2711

Das System-on-Chip (SoC) BCM2711 vereint nicht nur vier CPU-Kerne mit einer GPU, sondern enthält auch Controller für viele Schnittstellen.



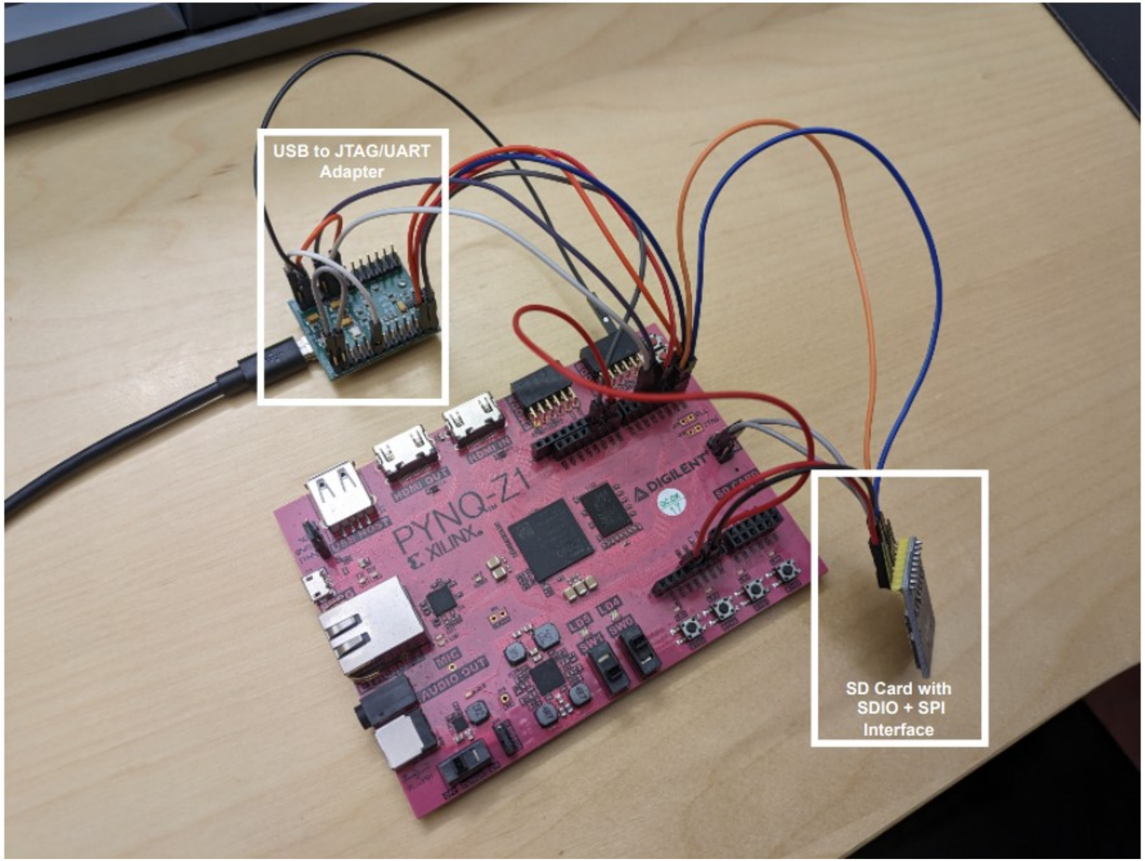
Are there differences in design process between these?

Digital IC design process (ASIC)



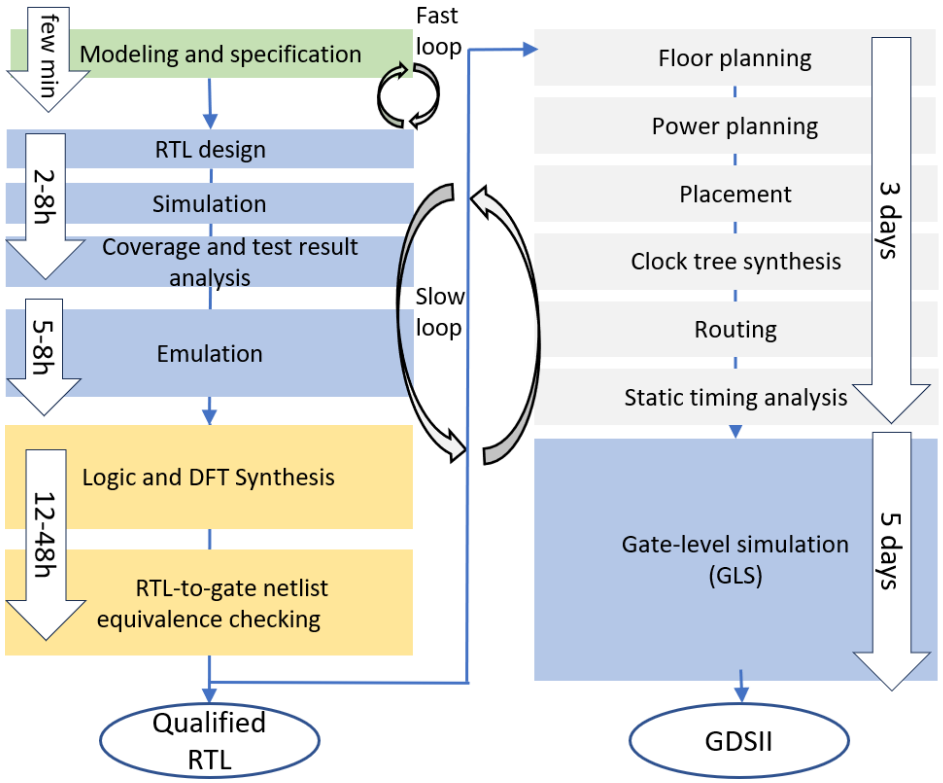
ASIC Prototyping on FPGA vs FPGA Design

- Clock source
  - ASIC: clock muxing and gating logic
  - FPGA: Ready clock tree
    - Gating structures not easy to implement
- Memories
  - ASIC: RTL models mapped to SRAM macros
  - FPGA: On-Chip SRAM cells, configured in Vivado
- Fast I/O interfaces
  - ASIC: Analog design projects (Custom macro)
  - FPGA: hard macros on chip



Digital IC tool flow

- When you go further, debugging becomes more painful
- Each change triggers a new loop iteration
- Commercial tools are expensive



The 2022 Wilson Research Group Functional Verification Study

- Research done biennially
- Focus is on verification, but summarising the relevant parts

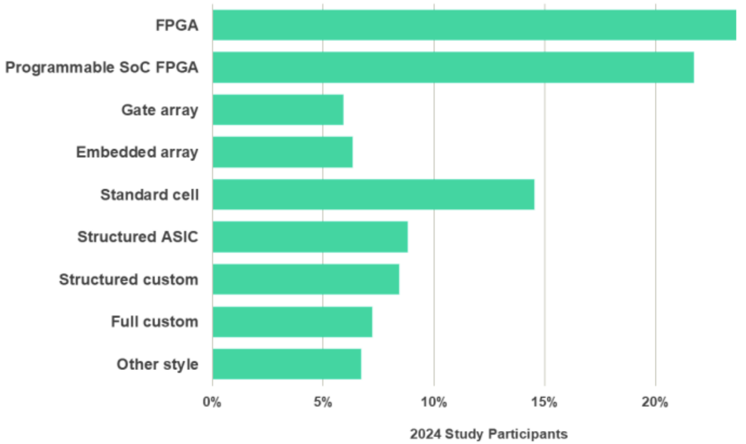


Figure 1. Study participants by targeted implementation.

2024 Wilson Research Group IC/ASIC functional verification trend report

[Prologue: The 2022 Wilson Research Group Functional Verification Study - Verification Horizons]

84%
One or more cores

63%
Two or more cores

10%
Eight or more cores

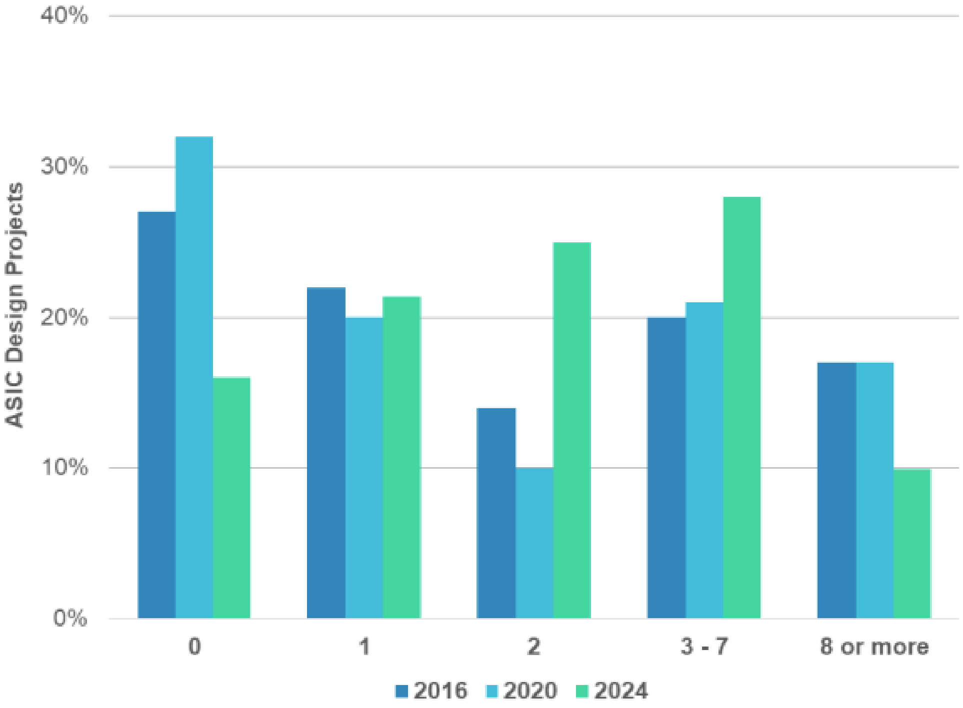


Figure 10. Number of embedded processor cores.

2024 Wilson Research Group IC/ASIC functional verification trend report

Designs with AI accelerators and RISC-V cores increasing

2024: 59%

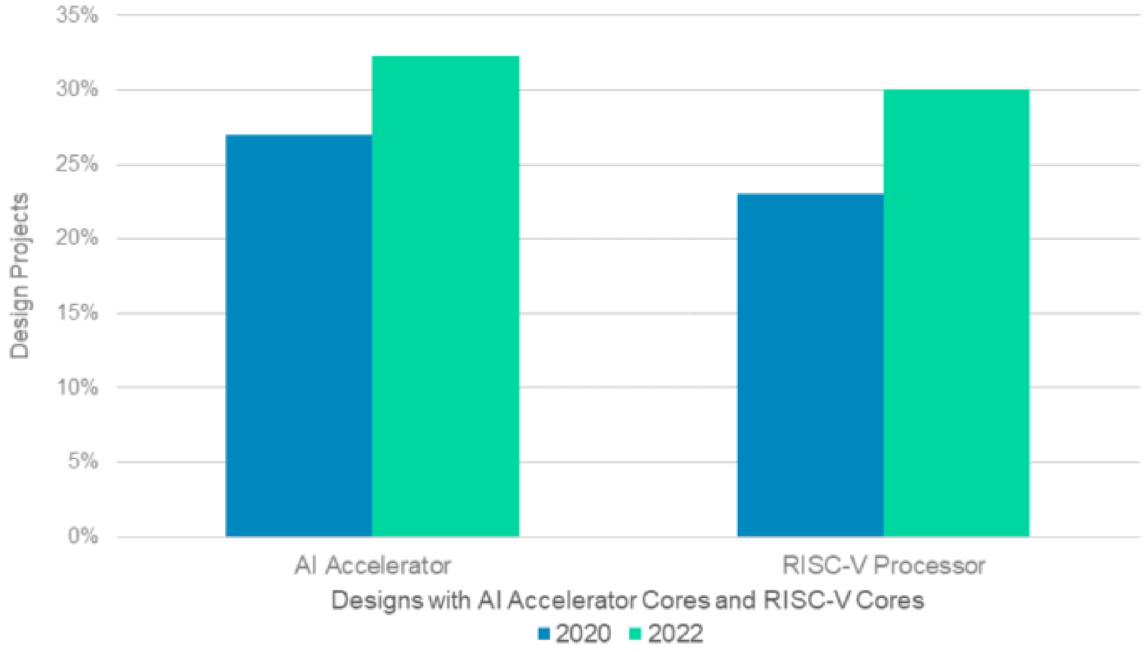
32%

ASICs with AI Cores

2024: 58%

30%

ASICs with RISC-V Cores

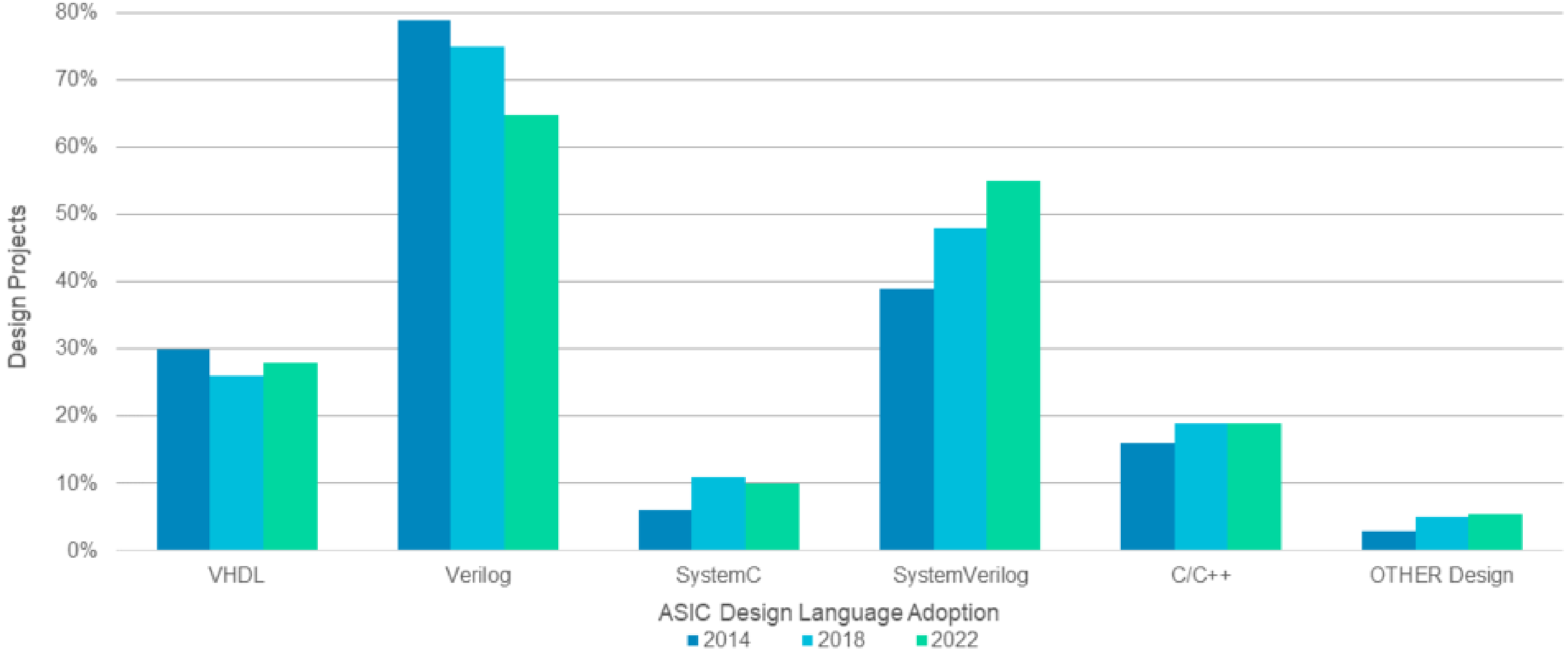


Source: Wilson Research Group and Siemens EDA, 2022 Functional Verification Study

SIEMENS

2024 Wilson Research Group IC/ASIC functional verification trend report

ASIC design language adoption (DUT)



* Multiple replies possible

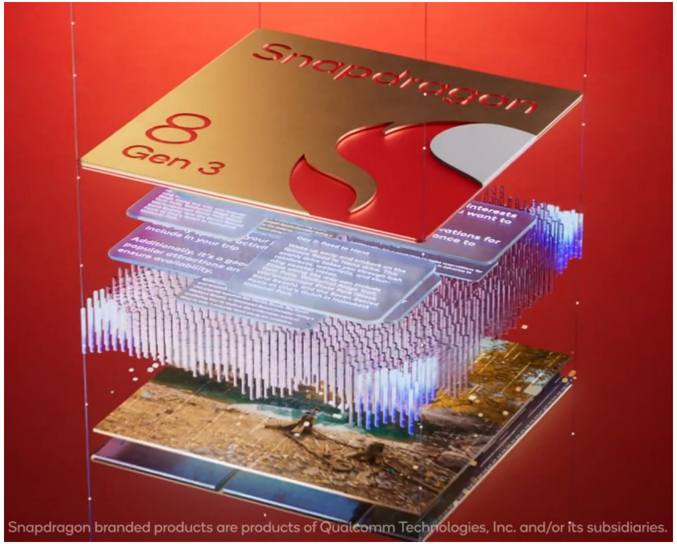
Source: *Wilson Research Group and Siemens EDA, 2022 Functional Verification Study*

SIEMENS

Tampereen yliopisto
Tampere University

Nvidia AD102 (RTX4090)

Snapdragon 8 Gen 3



Differences between designing these?

Design Targets

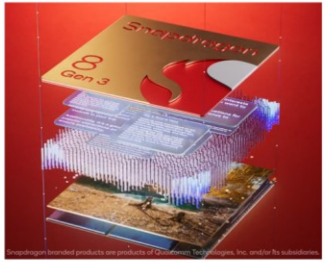
- Power challenges and area targets

- Mobile SoC: heterogeneous
  - Multiple different CPU cores and accelerators
  - Power optimized: battery-powered
    - Most of the chip sleeping while powered on
    - When to wake each element?

- GPU: homogeneous
  - Bandwidth limited: each element needs data written via PCIe
    - PCIe interfaces and GDDR memories evolving
  - Challenges: Internal interconnects, memory architecture
  - Power limit: Heat

Nvidia AD102 (RTX4090)

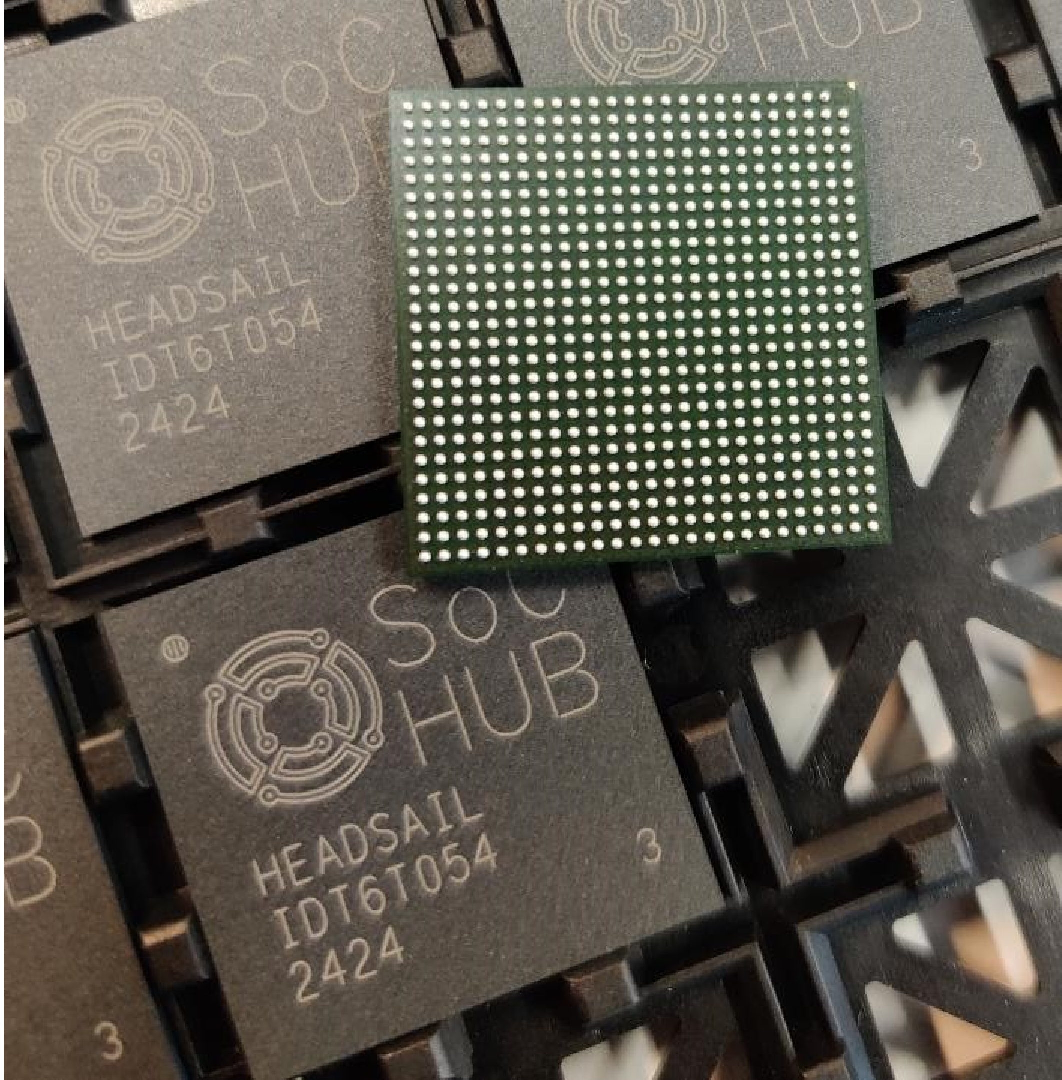
Snapdragon 8 Gen 3



SoC Hub

Finnish consortia and research center at Tampere University

- To date 120 contributors from 8 partners
- Objectives
  - New collaboration model
  - Big SoCs
  - Industry quality
  - SoC per year
  - Full design flow
  - Agile design approach

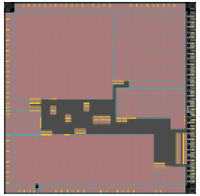
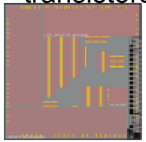
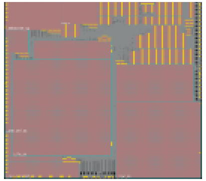
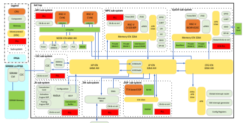


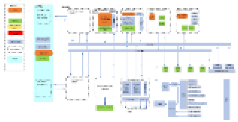
FLEXIBILIS CoreHW VLSI SOLUTION NOKIA
procemex Wapice CARGOTEC Tampereen yliopisto Tampere University

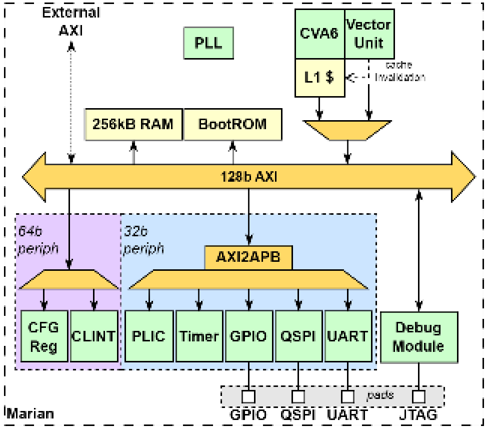
SoC Hub Chips

- Phase 1 completed: Ramp up fabless design competence
- Next: Lead and meet the (industrial) need

Pipe cleaning	IP development	SoC Template	IP development
Ballast 15mm2 256 PGA 130M transistors	**Tackle** 2x 4mm2 88 QFP 12M transistors	**Headsail** 25mm2 624 BGA 340M transistors	**Bow** (tapeout readiness)

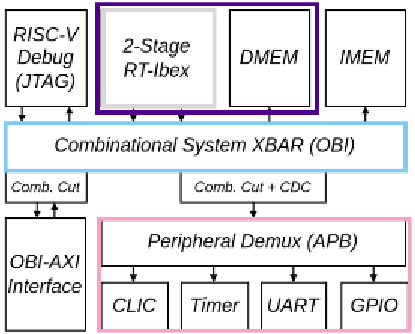









Marian Vector CPU

- Extends CVA6/ARA (RVV 1.0) with ratified vector cryptography extensions (Zvk) for AES, SHA, SM3 & SM4 bulk crypto
- First open-source vector core with Zvk



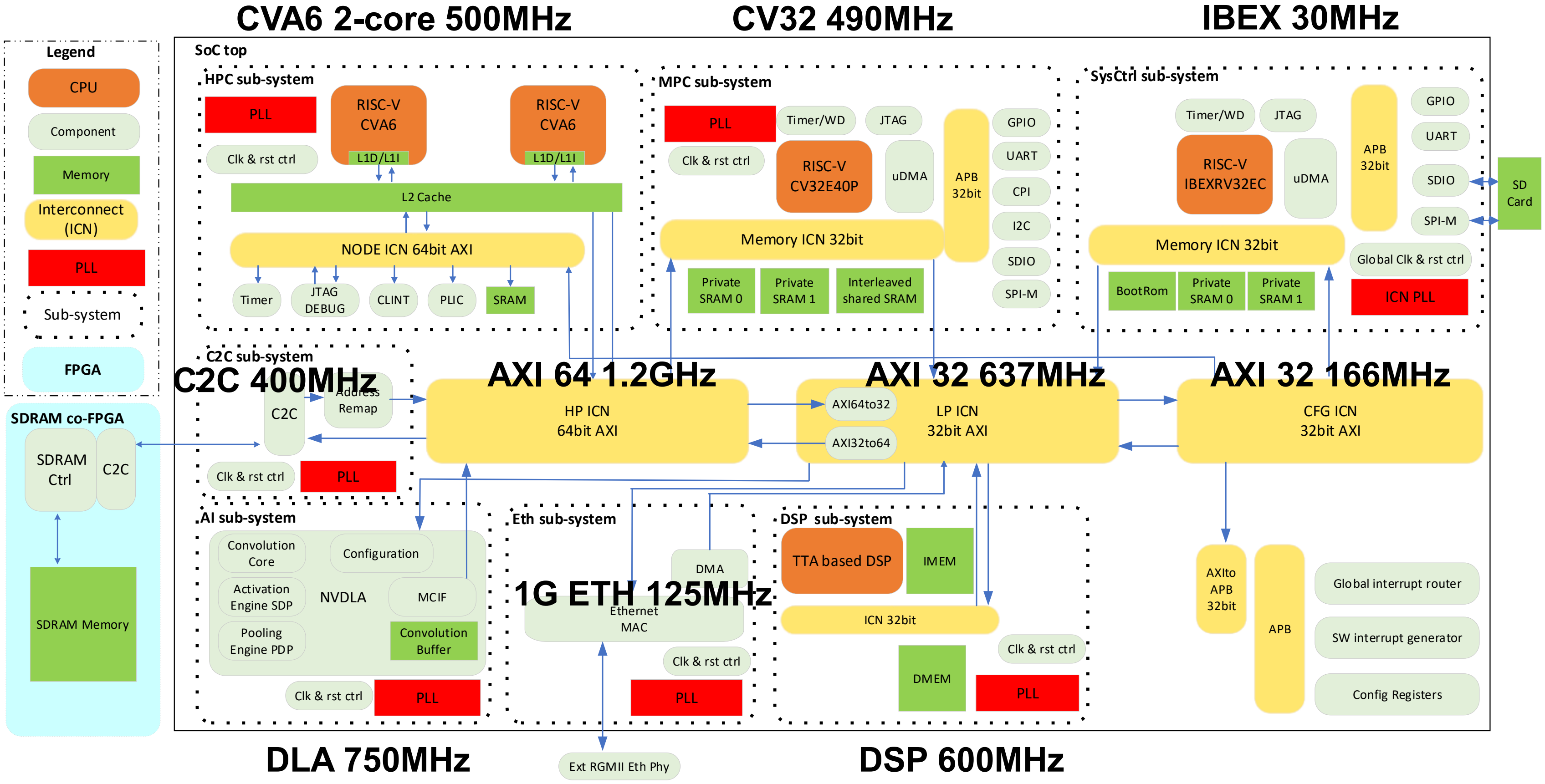
Real-Time Core

- IBEX fork
- Core-Local Interrupt Controller (CLIC) compliant
- Custom Hardware for accelerated context switch

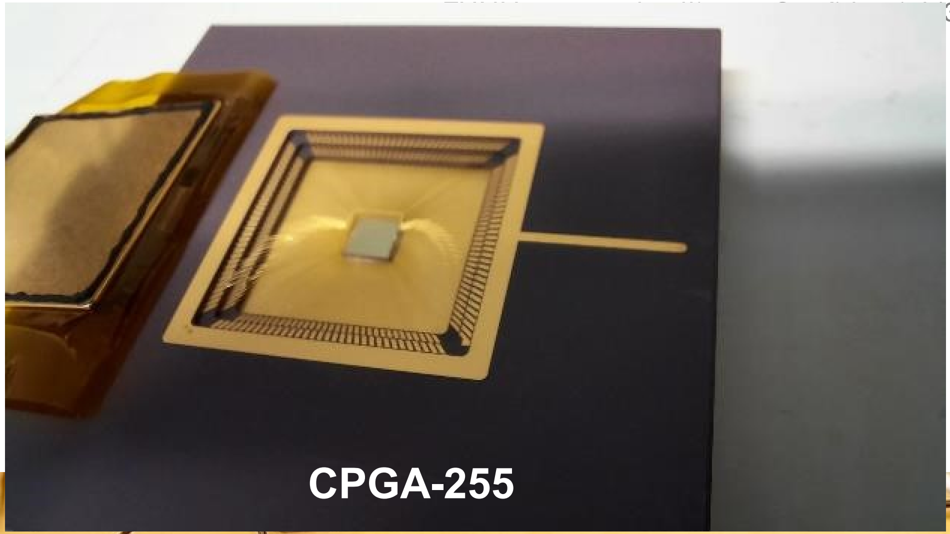
TSMC 22nm

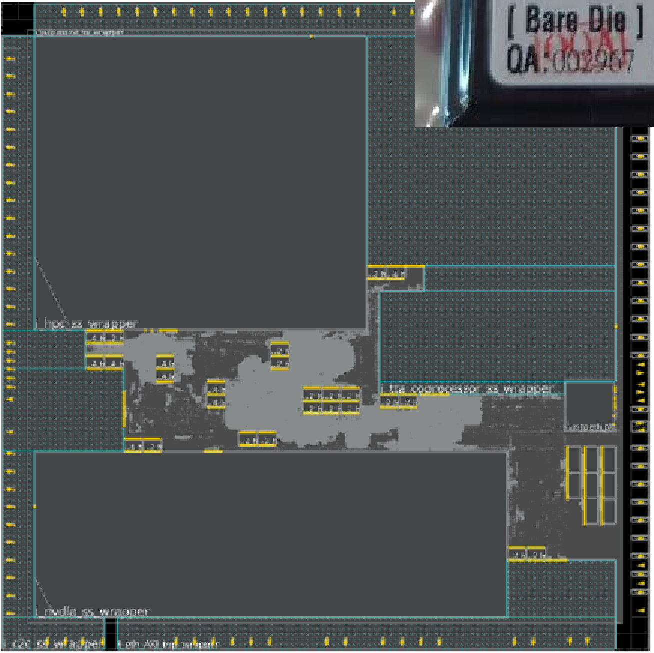
2021 2022 2023 2024 2025 2026 2027

Ballast architecture

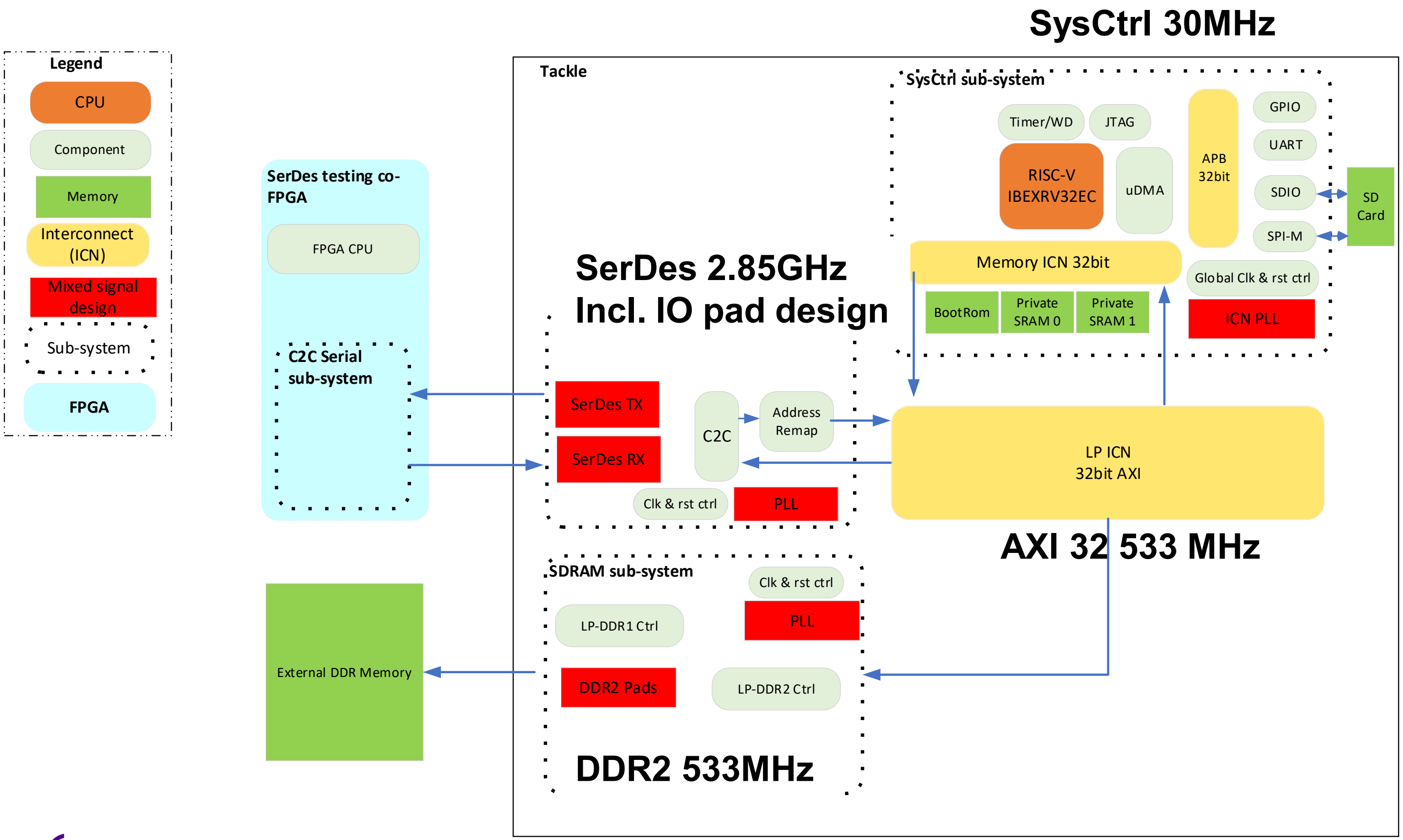


Ballast chip & board



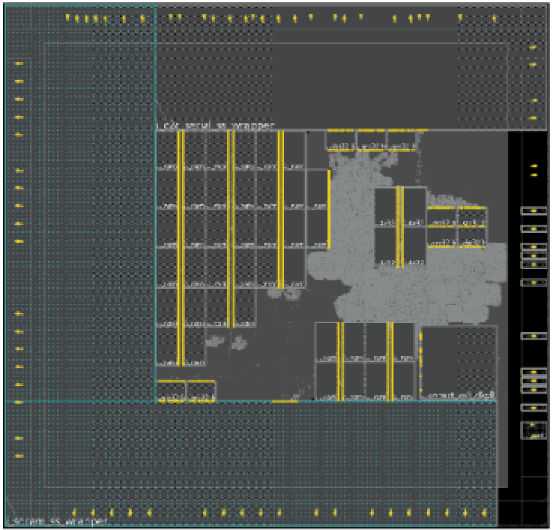


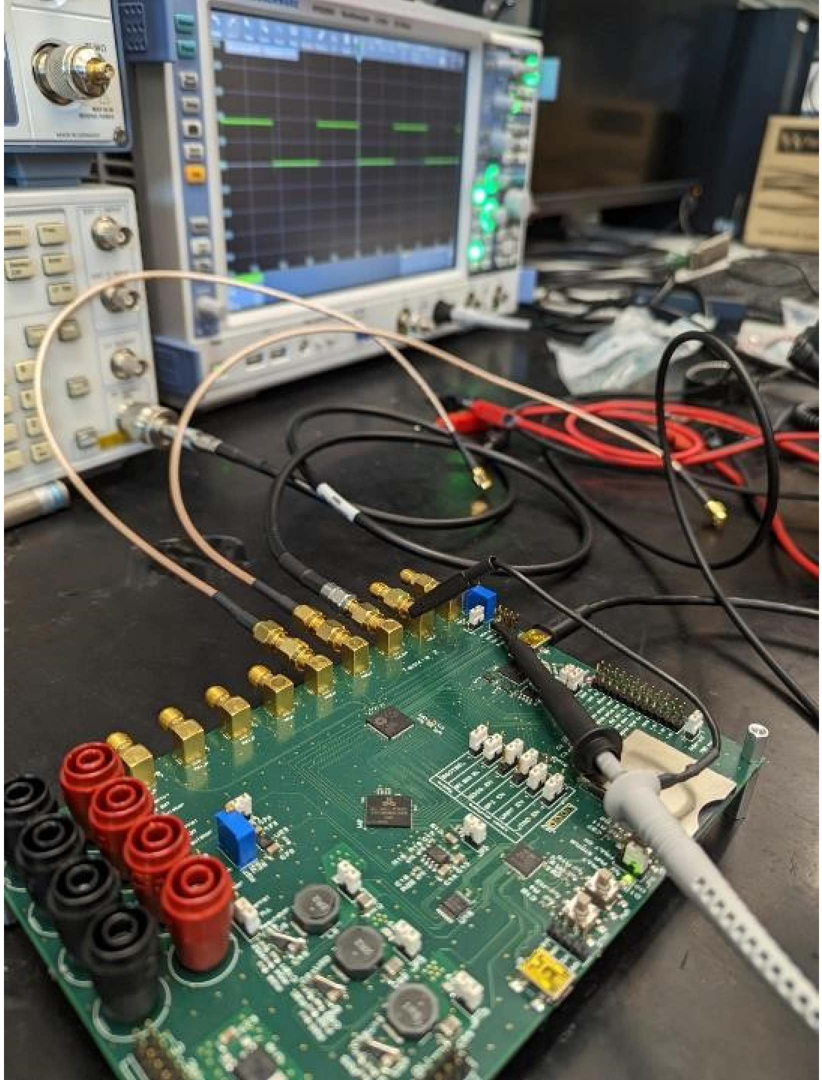
Tackle architecture



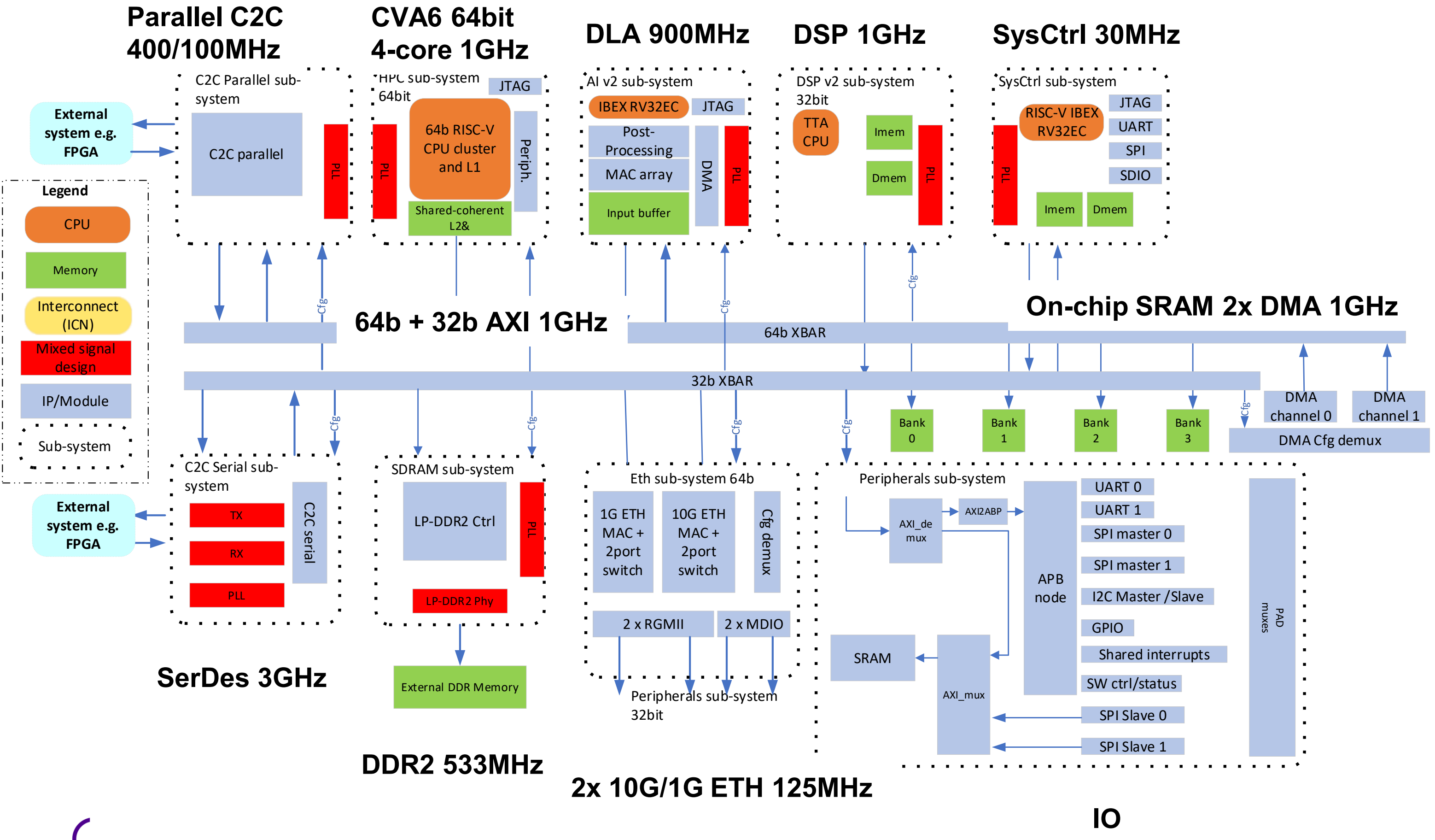
Tackle chips& board

QFP-88





Headsail Architecture



Technology
- TSMC 22nm ULL (low power)
- 25mm2 area
- 624pin BGA package
- 340M transistors
- Approx 3MB of internal SRAM
- up to 3GHz PLL (clock)

RISC-V CPU sub-systems
- 4x 64b 6 stage RISC-V CVA with shared 512kB L2$
- 32b 2-stage IBEX RV32IMC

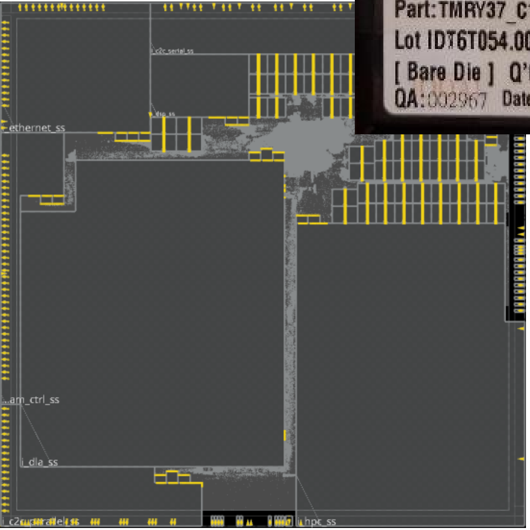
Accelerators
- Deep-Learning Accelerator: 512kB buffer, IBEX control CPU, 64x64MAC array
- DSP: VLIW-like core based on the Transport Triggered Architecture (TTA), openasip.org

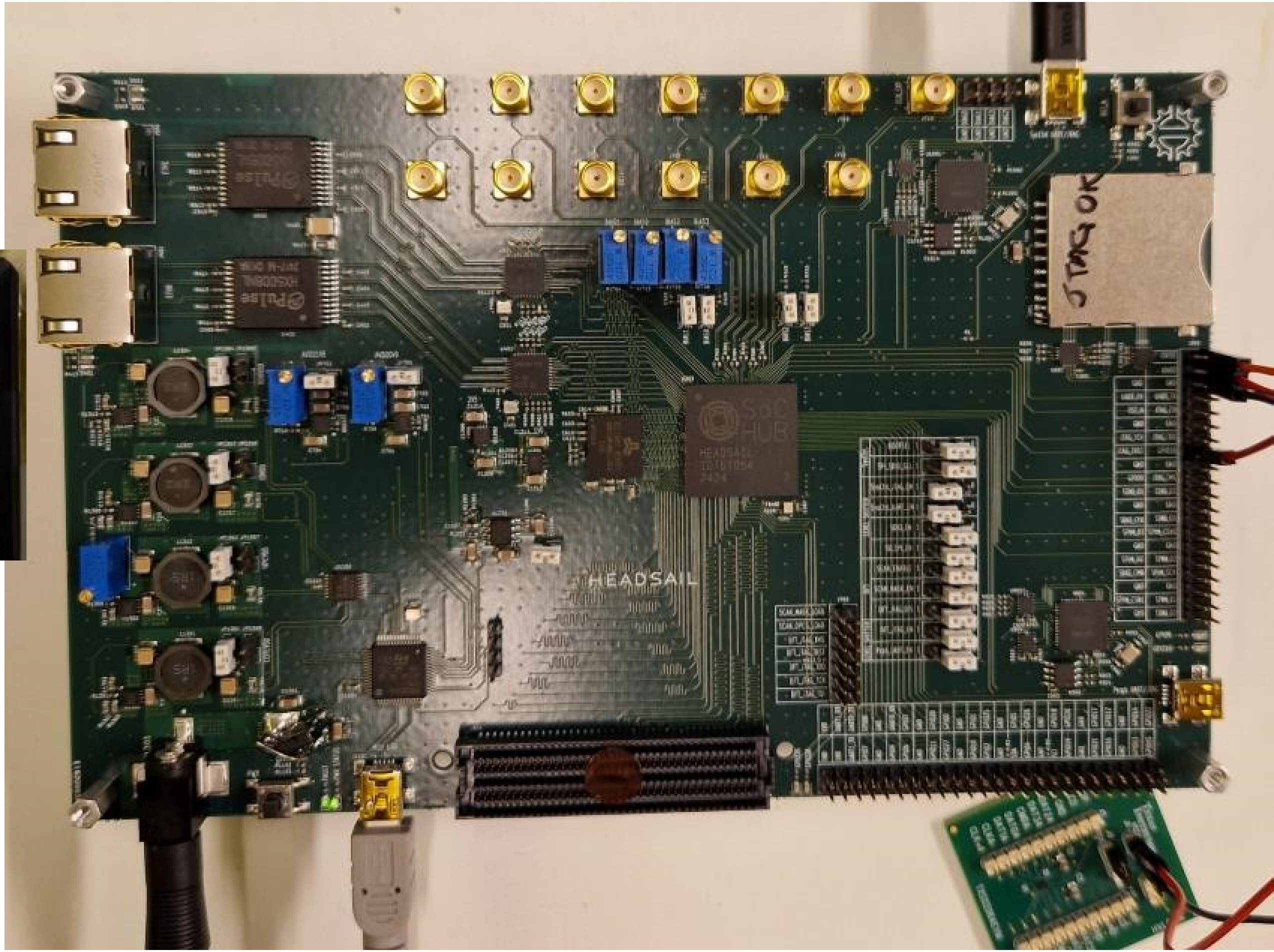
Interfaces
- **QSPI, UART, SDIO, GPIO**
- **Ethernet** 10Gbps MAC,2x 1Gbits/s
- **Chip-to-Chip parallel**: 16bit wide phy. With 3.2Gbits/s unidirectional bandwidth
- **Chip-to-Chip Serial.** SerDes with custom Clock Data Recovery (CDR) & LVDS pads
- **LP-DDR2.** 533MHz. 16bit DDR databus
- **AXI4** crossbar interconnect 64b and 32b

Tampereen yliopisto
Tampere University

Headsail chip & board

BGA-624



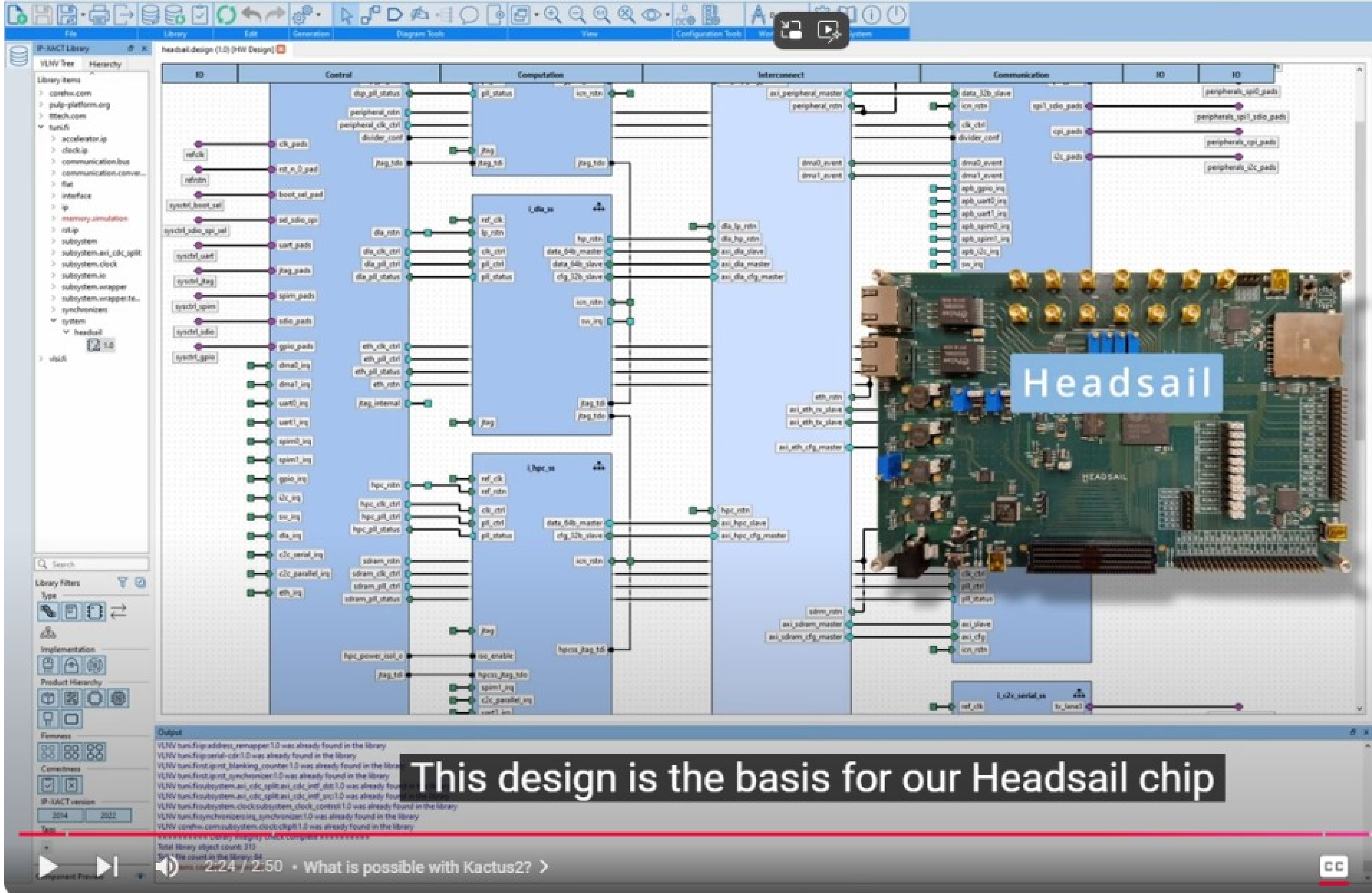


SoC details

	Ballast		Tackle		Headsail	
Sub-system	Freq.	Area (inc. mem.)	Freq.	Area (inc. mem.)	Freq.	Area (inc. mem.)
HPC (CVA6)	500MHz	5,3mm^2 (2x cores)	NA	NA	1GHz	7mm^2 (4x cores)
MPC (CV32E40P)	500MHz	2,5mm^2	NA	NA	NA	NA
SysCtrl (IBEX)	30MHz	0,35mm^2	30MHz	0,32mm^2	30MHz	0,42mm^2
DSP	600MHz	0,95mm^2	NA	NA	1GHz	0,74mm^2
C2C Parallel	400MHz, los 100MHz	1mm^2	NA	NA	400MHz, los 100MHz	1mm^2
C2C Serial	NA	NA	2,85GHz	0,3mm^2 (excl. analog macros)	3GHz	0,4mm^2 (excl. analog macros)
AI: NVDLA	750MHz	2,6mm^2	NA	NA	NA	NA
AI: DLA	NA	NA	NA	NA	900Mhz	9,4mm^2
1G ETH	125MHz	0,7mm^2	NA	NA	NA	NA
2x1G ETH	NA	NA	NA	NA	125MHz	1,5mm^2
LP-DDR2 SDRAM	NA	NA	533MHz	1,5mm^2 (excl. analog macros)	533MHz	1,5mm^2 (excl. analog macros)
ICN+ DMA+ Shared SRAM	1200 /637 /166MHz	2,37mm^2 (No DMA nor SRAM)	533MHz	0,9mm^2	1Ghz	3,8mm^2
IC package	CPGA-255		QFP-88		BGA-624	

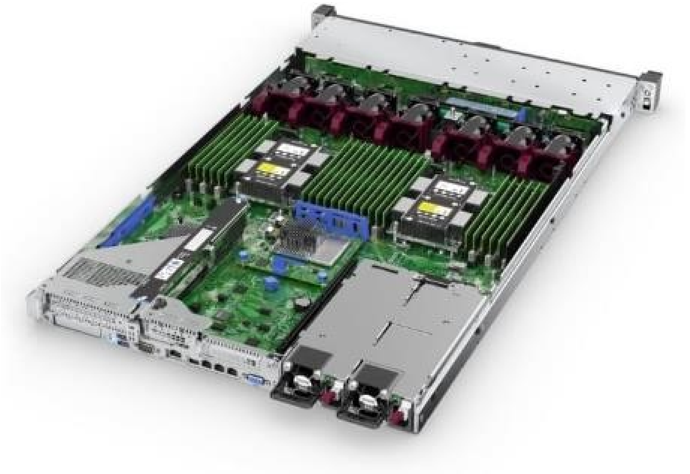
SoC Hub tools

- IP-XACT / Kactus2 for modeling the architecture and memory maps
  - Code generation for RTL and FW development
  - 226 IP-XACT XML documents
- Openasip.org DSP generator tools
- Keelhaul tool for verifying memory maps @SW
- Cadence tools for physical design



SoC Hub computing resources

- Hardware
  - 144 cores (6x 24-core Xeon-G 6248R 4GHz)
  - 4.5TB RAM
  - 16 TB SSD
- Virtual servers for
  - RTL design and simulation
  - Physical design
  - Gitlab CI pipeline runners
- Example run times
  - physical design from RTL to DRC checked GDS-II: **1-64 hours**
    - Depends on sub-system
    - Executed ~100 times per subsystem x 10 subsystems
  - Several months of CPU time per chip
    - Headsail ~50k hours / thread / full run



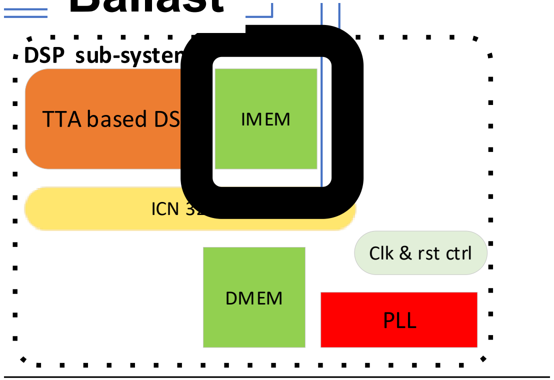
Movie bloopers

Ballast: DSP instruction memory enable signals inverted (human mistake with repositories)

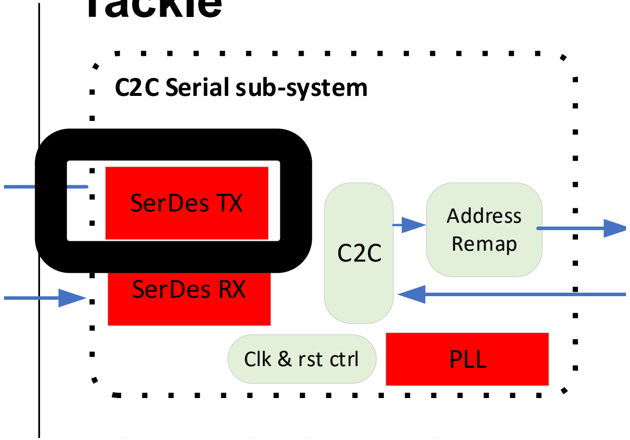
Tackle: SerDes Rx not working (last moment changes before tapeout)

Headsail: CVA6 is not able to boot Linux (L2 cache bug)

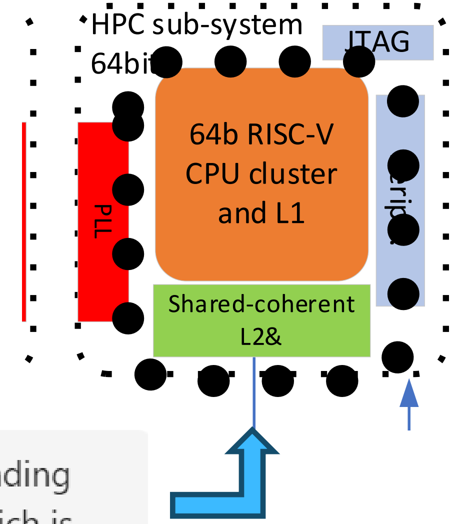
Ballast



Tackle



Headsail

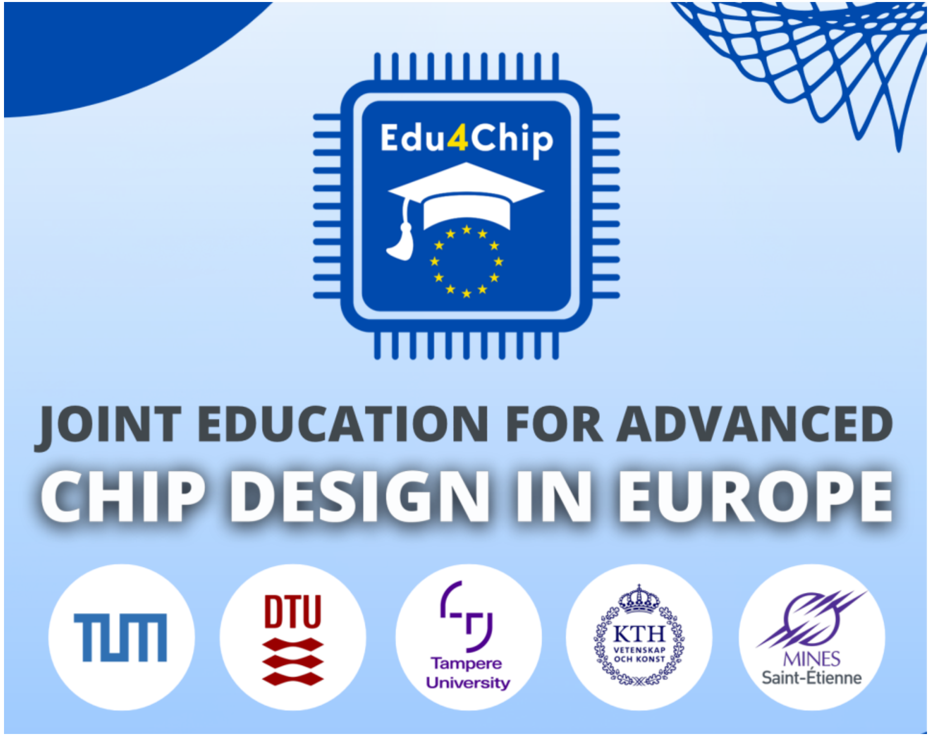


AK

Yes, the openSBI runs to completion...but fails just before loading the payload...The instruction being skipped here is MRET which is one of the two bugs we are trying to figure out now

Oct 29, 2024

Edu4Chip



Developing aligned Master's course programs for **Advanced Chip Design**

The full chain from **RTL Design** to **Tape-Out** and waking up your own chip

Tampere University: The new **Advanced Studies in System-on-Chip Design** study module

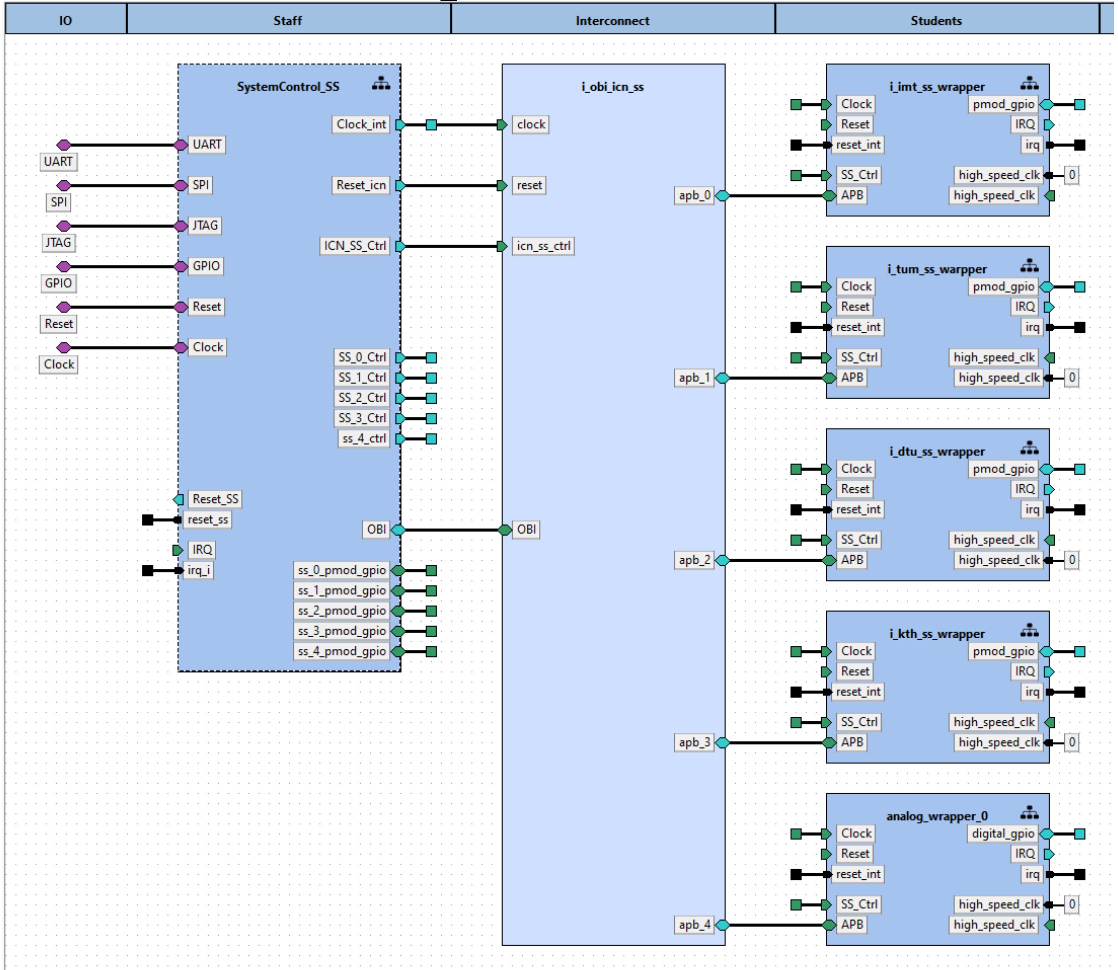
https://edu4chip.github.io/

Edu4Chip - Joint Education for Advanced Chip Design in Europe is funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the European Health and Digital Executive Agency (HADEA). Neither the European Union nor the granting authority can be held responsible for them.

Funded by the European Union

EDU4CHIP ”Didactic” SoC template

- Staff area
  - SysCtrl
  - SD card
  - Shared Ios: UART, GPIO
- Student area
  - Subsystems to be plugged in
  - APB interconnect
  - GPIO multiplexed
- Open source
  - IP-XACT model
  - Subsystem interface template and RTL



Tampereen yliopisto
Tampere University

COMP.CE.250
System-on-Chip Design

Getting Started

Arto Oinonen

COMP.CE.250 System-on-Chip Design

Learning outcomes:

"After completing the course, the student can work as part of a SoC subsystem design team.

They know the common internal interconnects and external interfaces, and the usual phases of the design project. They can analyze their design choices in terms of power, performance, and area."

Our target:

- Deepening the themes from Logic Synthesis, but not that much new content
- Practical experience on common steps & problems in modern SoC design

Side benefit:

- A course SoC that we could tape out to produce our own physical ASIC
- COMP.CE.510 Chip Implementation would continue from this design all the way to GDSII that can be sent to the foundry *(not promised on the first implementations, yet)*

Course Staff

- Arto Oinonen
  - Responsible teacher
  - arto.oinonen@tuni.fi

- Antti Nurmi
  - Lectures
  - Exercise project

- other lecturers + project work staff

- Contact:
  - Mattermost channel preferred

Tentative schedule

Lectures:

- 1st Period: Lectures
- 2nd period: Special topics
  - By experts, on their expertise
  - Tools
  - Design challenges
  - Applications

Exercises:

- Design project starts in February

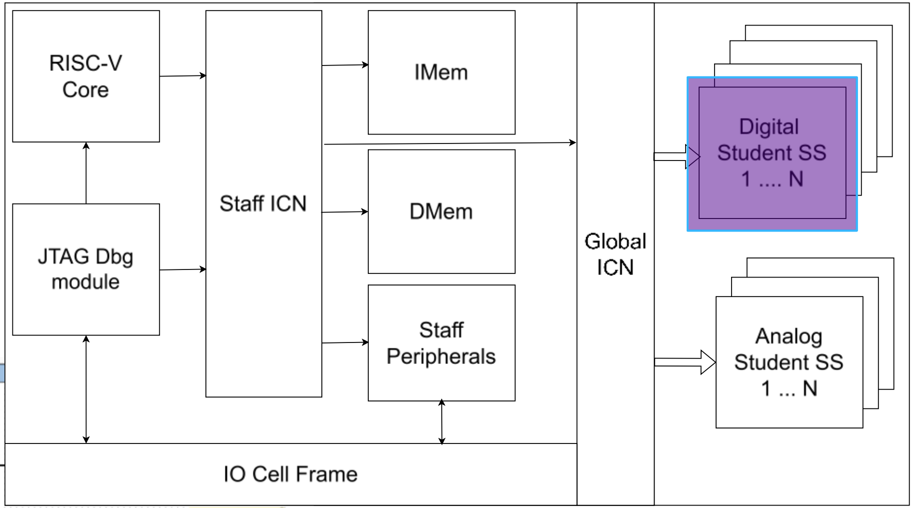
Up to date schedule on Plussa course front page

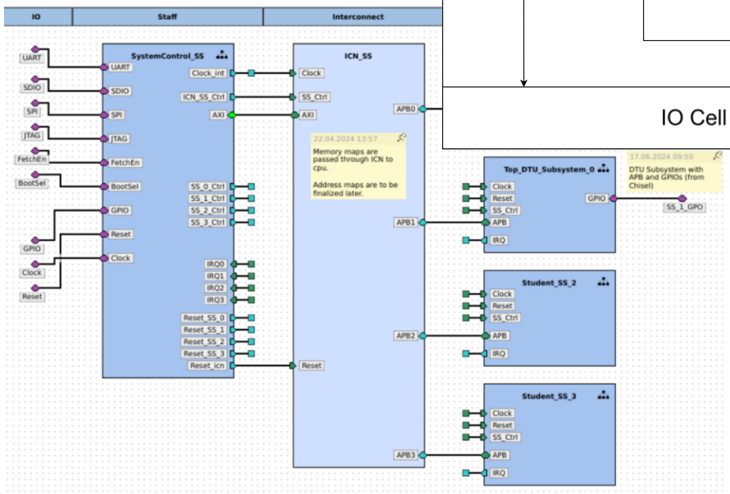
wk	Wed 14-16	Lecture	Exercise	Ex opens	Deadline
3	14/01/2025	Course info			
4	21/01/2025	SystemVerilog for Design	SV Introduction	19-Jan	08-Feb
5	28/01/2025	SoC Survey	SoC Survey		
6	04/02/2025	Computer Architecture for System-on-Chip Design			
7	11/02/2025	Interconnects	EX0: Didactic intro	11-Feb	
8	18/02/2025	Exercise Project Introduction & Practical SoC Development	Exercise project	18-Feb	
9					
10	04/03/2025	Special topic			
11	11/03/2025	Special topic			
12	18/03/2025	Special topic			
13	25/03/2025	Special topic			
14	01/04/2025	easter 1. - 7.4.	easter 1. -7.4.		
15	08/04/2025	Special topic			
16	15/04/2025	Special topic			
17	22/04/2025	wrapup			
18	29/04/2025	EXAM WEEK			
19	06/05/2025	EXAM WEEK			

Exercise project

- You will integrate your group's own IP on the Didactic SoC platform

- More details when it's time to start





Passing the course

- SoC Survey: must be passed
- Exercise project: 50% of the grade
- Exam: 50% of the grade
  - Electronic exam at the end of period 4

- 50p -> 1
- 60p -> 2
- 70p -> 3
- 80p -> 4
- 90p -> 5

Prerequisites

1. **Basic knowledge of digital design with HDL**
   – VHDL (or Verilog) experience
   ➢ *Understand the challenges*
   ➢ *Understand SystemVerilog concepts*
   ➢ *COMP.CE.240 Logic Synthesis or equivalent skills*

2. **Recommended: (RISC-V) CPU architecture**
   ➢ *COMP.CE.130 Computer Architecture or equivalent*

First task: SoC Survey 27.1. - 30.1.

1. Sign up for a group in Moodle
   - Exercises are done in 2-3 person groups

2. Summarize the content of a GitHub repository assigned for your group
   - 5-10 minutes: 2-3 slides is enough

- Options available:
  - Open-source SoC platforms,
  - CPU (RISC-V) cores,
  - Open PDKs,
  - Related tools

- Results are presented on **lecture 28.1.** and **exercise sessions on Monday 26.1. and Thursday 29.1.**
  - Registrations for sessions in Moodle

- Assignment instructions in Plussa

Next week: SystemVerilog for Design

- The design-oriented properties of SystemVerilog language
- No exercise sessions yet, but the FPGA lab is reserved for you
  - Tools for studying for the SoC Survey
- Optional SV introduction exercise
  - Shared with SoC Verification: not required twice