Tampereen yliopisto
Tampere University

COMP.CE.250
System-on-Chip Design

Wrap up

Arto Oinonen

COMP.CE.250 System-on-Chip Design

Learning outcomes:

"After completing the course, the student can work as part of a SoC subsystem design team. They know the common internal interconnects and external interfaces, and the usual phases of the design project. They can analyze their design choices in terms of power, performance, and area."

Our target:

- Deepening the themes from Logic Synthesis, but not that much new content
- Practical experience on common steps & problems in modern SoC design

Side benefit:

- A course SoC that we could tape out to produce our own physical ASIC
- COMP.CE.510 Chip Implementation would continue from this design all the way to GDSII that can be sent to the foundry *(not promised on the first implementations, yet)*

Course content

Lectures:

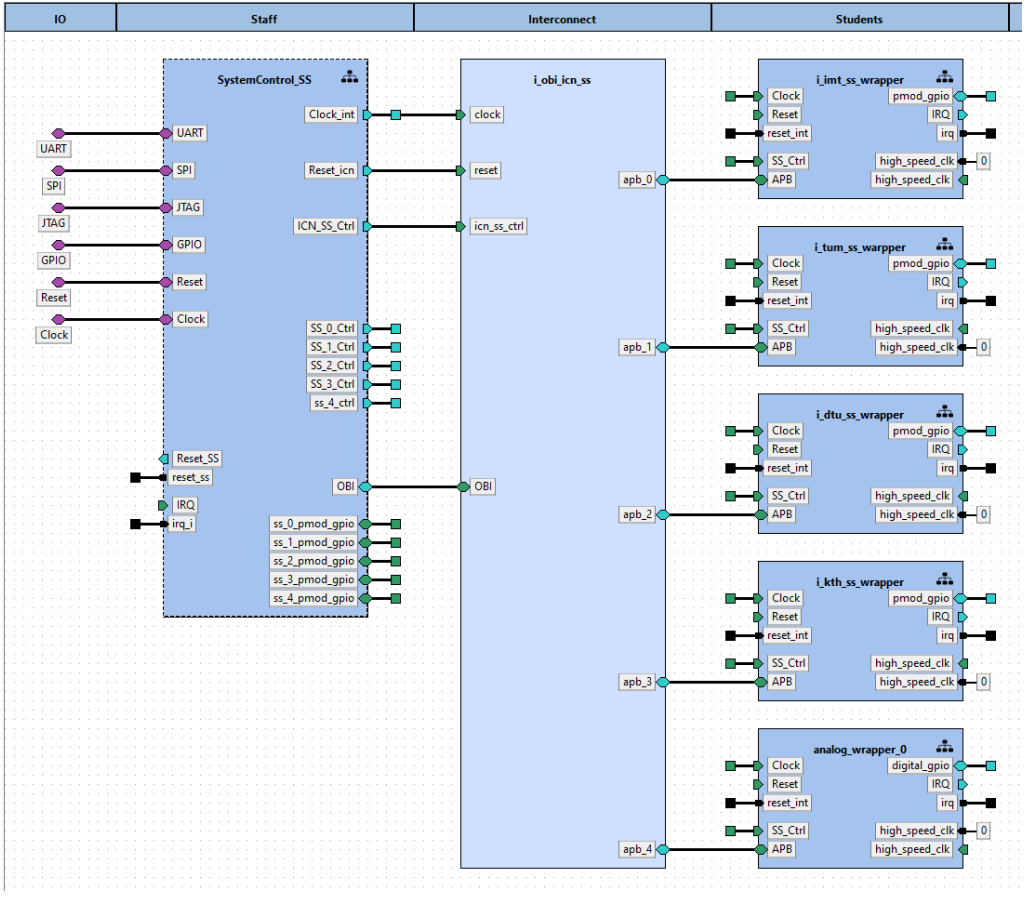
- 1st Period: Lectures
  - SystemVerilog
  - Computer Architecture
  - Interconnects
- 2nd period: Special topics
  - *”By experts, on their expertise”*

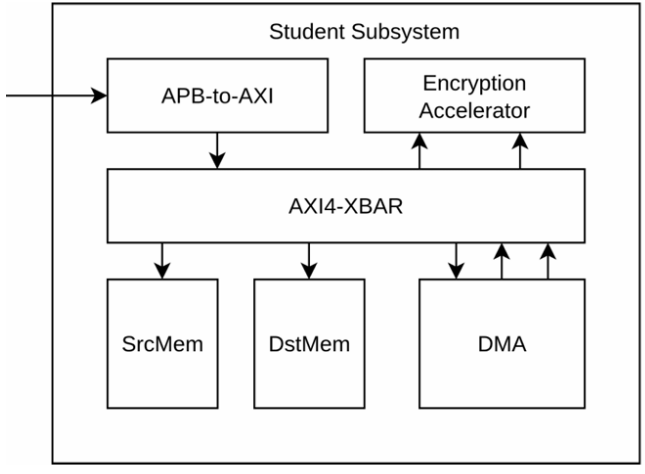
Exercises:

- SoC Survey
- (SystemVerilog intro)
- AXI DMA project

wk	dates	lecture Wed 14-16	exercise Mon 14-16 and Thu 14-16	deadline
3	12.1. - 18.1.	Course info		
4	19.1. - 25.1.	SystemVerilog for Design		
5	26.1. - 1.2.	SoC Survey	SoC Survey	30.1.
6	2.2. - 8.2.	Computer Architecture for System-on-Chip Design	Introduction to SystemVerilog	8.2.
7	9.2. - 15.2.	Interconnects	Ex0: Hello, Didactic	22.2.
8	16.2. - 22.2.	Exercise Project Introduction & Practical SoC Development	Ex0: Hello, Didactic	
9	23.2. - 1.3.	**EXAM WEEK**		
10	2.3. - 8.3.	Special Topic: FPGA Architectures and Applications (Arto)	Ex0: Hello, Didactic	
11	9.3. - 15.3.	**No lectures**	Ex1: Design an AXI-DMA	
12	16.3. - 22.3.	Special Topic: Power & Clock Domains (Arto)	Ex1: Design an AXI-DMA	
13	23.3. - 29.3.	Special Topic: Predictable Computer Architecture (Antti Nurmi)	Ex1: Design an AXI-DMA	
14	30.3. - 5.4.	**Easter 1. - 7.4.**	**Easter 1. - 7.4.**	
15	6.4. - 12.4.	Special Topic: GPU Architecture (Jakub Žádník)	Ex1: Design an AXI-DMA	
16	13.4. - 19.4.	Special Topic: SoC Security (Tom Szymkowiak)	Ex2: Documenting the DMA	
17	20.4 - 26.4.	Wrap up	Ex3: System-level Integration (bonus)	
18 19	27.4. - 10.5.	**EXAM WEEK**		

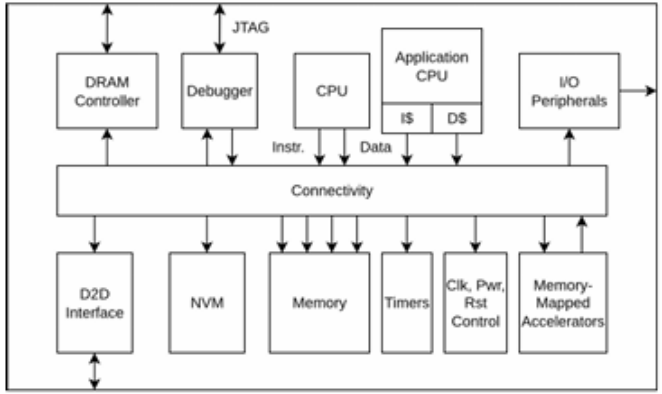
Exercise project

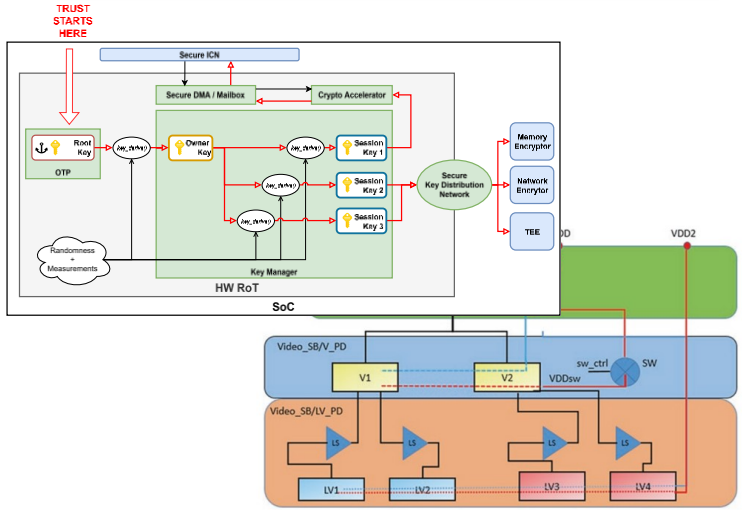




Not only RTL design

- **SW running on HW** -> Microarchitecture
- **Interconnect** -> protocols, congestion, coherency
- **Clock domains** -> CDC structures
- **Power domains** -> UPF
- **Security** -> RoT, secure boundaries -> secure boot
- **Real-time latency requirements ->** rethinking the architecture
- **Bandwidth and performance ->** Memory locations, caches





SoC Survey

Monday 26.1. at 14:15 (TC217)

14
Muntjac
★1

Pulpissimo

★1

16
Morty&Bender
★1

Wednesday 29.1. at 14:15 (TB206)

13
Black-Parrot
★0

18
Chisel
★0

12
CVA6
★0

7
TinyTapeout
★0

IHP-Open-PDK (23)
★0

Thursday 29.1. at 14:15 (TC217)

11
Ibex
★0

22
Skywater PDK
★0

17
Kactus2
★0

10
Chipyard
★0

5
Caravel
★0

19
OpenROAD
★0

3
Carfield
★0

Feedback on content

- Prototype course: to be improved for next year
  - Thank you for participating!

- **Lectures:**
  - Did the content feel relevant?
  - What would you add?
  - What would you remove?

- **Exercise project:**
  - challenges with the redesigned exercise project
  - ➢ Open the project at the beginning of the course next year
  - ➢ Extend the target:
    - ➢ FPGA prototyping
    - ➢ synthesis results?
    - ➢ PPA analysis
  - ➢ Your thoughts?

Course feedback in
https://norppa.tuni.fi/
- Open 27.4. – 17.5.

➢**+1 point to the Exam**

Captain Hindsight:
- *JIT compilation is not the right course development strategy*

Passing the course

- **SoC Survey presentation: all groups ok**
- *(SystemVerilog intro: optional)*

- **Hello, Didactic: 5**
- **AXI-DMA: 30**
- **Documentation: 15**
- **Integration: 20 (bonus)**

- Exercise project: 50% of the grade

- Exam: 50% of the grade

Grading

- Exercise project: 50 points
  - +20 for the Lab 3
- Exam: 50 points

- Sum: 100 points (absolute maximum 120)
  - Minimum: 50 points

•50p -> 1
•60p -> 2
•70p -> 3
•80p -> 4
•90p -> 5

Exam in May 2026

- Exam: https://exam.tuni.fi

- Exam period open 27.4. – 17.5. (3 weeks)
  - 1st submission must be graded before the next try
  - Three windows: second one in June and the third in the Fall
  - Three possible attempts

- Exam implementation in Sisu
  1. Sign up for exam in Sisu
  2. Reserve your time in Exam

Exam principles

- To check that you know the concepts, terms and methodologies
- To check that you understand what you did in the exercises

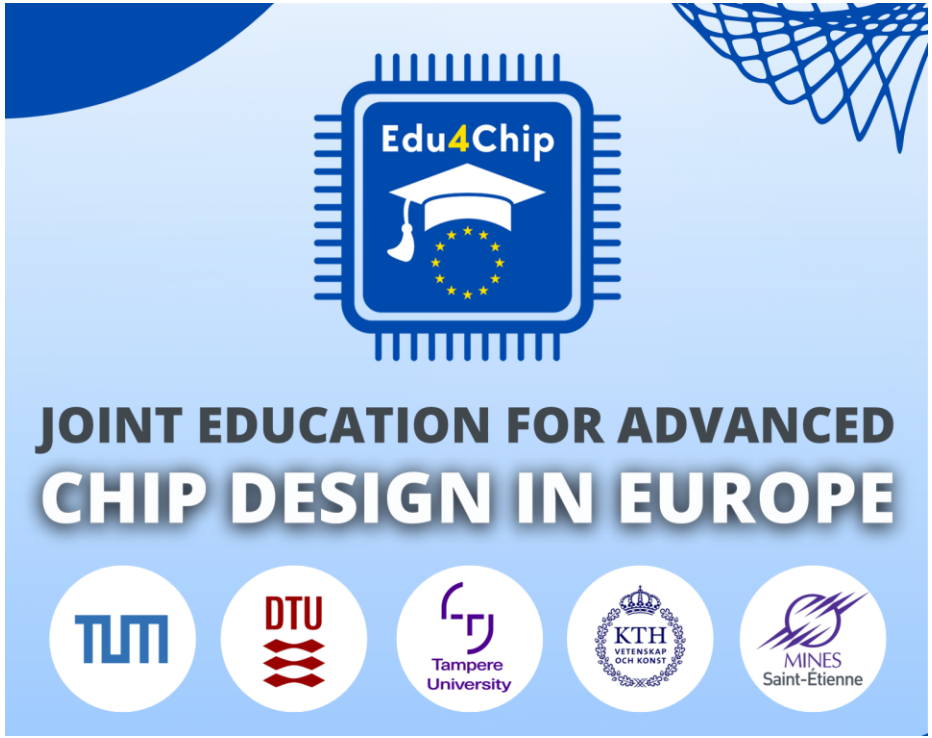
EXAM

1. Lecture content (18 points)
   - Small questions (~50 words)
   - The main topics on each lecture
   - Questions randomized form a pool

2. Design/analysis task (32 points)
   - ~~*Ready SystemVerilog code to analyze and implement?*~~
   - *Block diagram to analyze, partition & complete?*
   - *Architecting your own SoC and analyzing your design choices?*
   - *Anything else, but be prepared to think on SoC architecture level*

   ➢ ***PPA***

Edu4Chip



Developing aligned Master's course programs for **Advanced Chip Design**

The full chain from **RTL Design** to **Tape-Out** and waking up your own chip

Tampere University: The new **Advanced Studies in System-on-Chip Design** study module

https://edu4chip.github.io/

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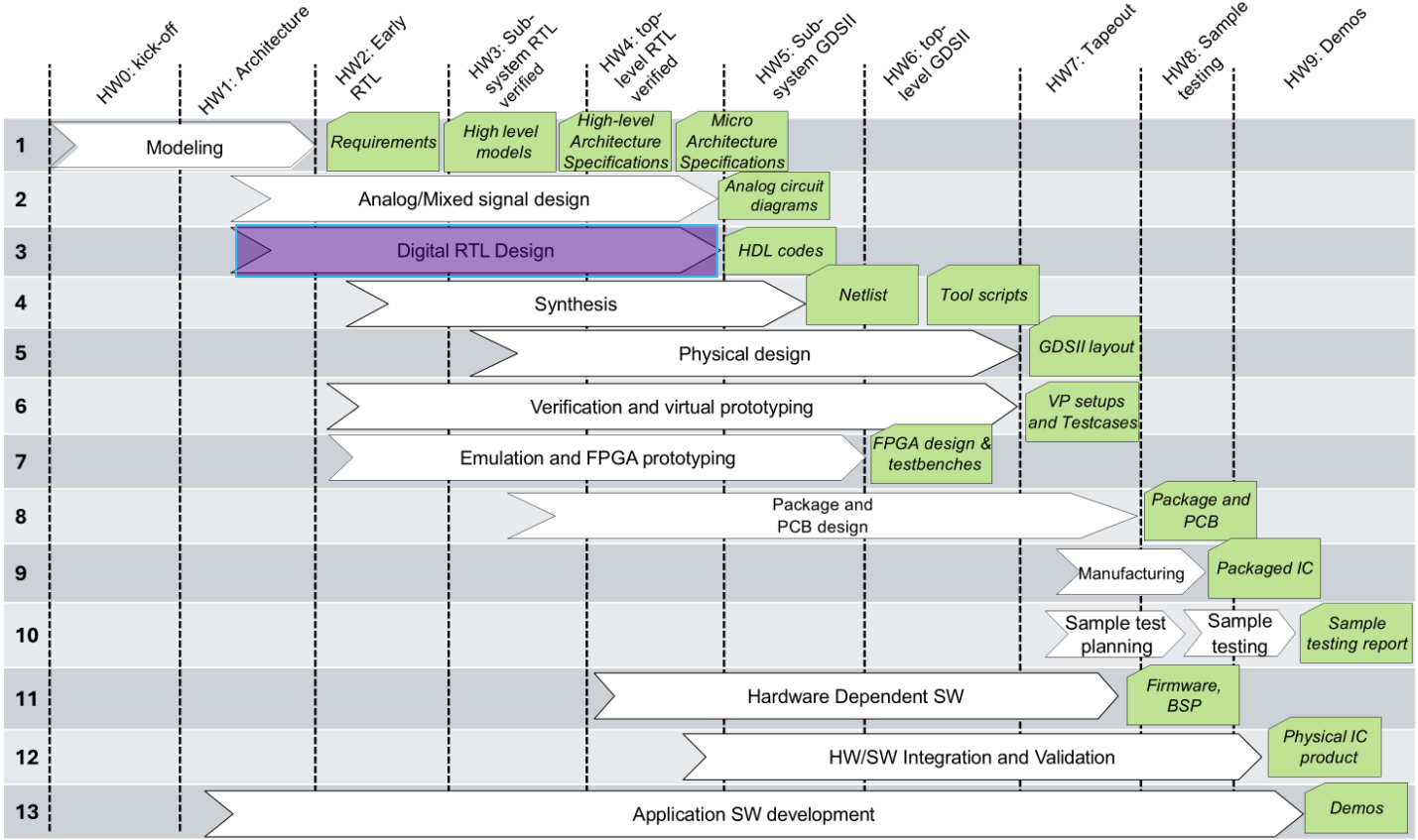
Digital IC design process (ASIC)



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SoC Design curriculum thoughts?

Arto Oinonen

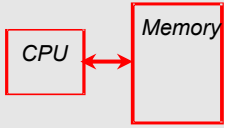
TUNI Luotettava kumppani — Confidential (3Y)

Computer engineering studies 2026

COMP.CE.100 Introduction to Embedded Systems

Bare-metal ARM programming

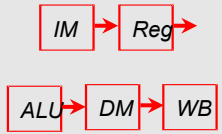
”Alien game” project



COMP.CE.130 Computer architecture

Processor’s data & control path, pipeline

”Processor simulation work”



COMP.CE.350 Parallel Computing

High perf. SW on MC, SIMD, GPGPU

”Real time physics simulation"

OpenMP

OpenCL

COMP.CE.460 Embedded Linux Drivers

Real-time Linux on SoC-FPGA

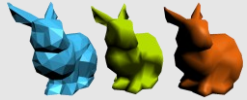
”Interrupt flooding” work

yocto

COMP.CE.430 Computer Graphics

3D Graphics and GPU usage

"Basic 3D game"



COMP.CE.340 Dependable Embedded Systems

Rust and RTIC

”Real-time app on SoC-FPGA RISC-V”

COMP.CE.470 Video Compression

HEVC and VVC video encoding

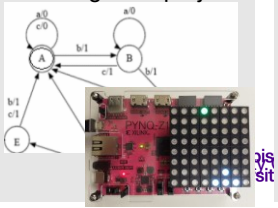
”Encoder implementation” work

ULTRA VIDEO GROUP

COMP.CE.200 Digital Design

Combinational and sequential logic, EDA Tools

”Alien game” project



COMP.CE.240 Logic Synthesis

VHDL synthesis for FPGA

”Audio synth”

```
CASE current_state IS
   WHEN get_1 =>
      IF (napit_in(0) = '1') THEN
         next_state <= store_1;
      ELSE
         next_state <= get_1;
      END IF;
   WHEN store_1 =>
      next_state <= get_2;
   WHEN get_2 =>
      IF (napit_in(0) = '1') THEN
         next_state <= store_2;
      ELSIF (napit_in(3) = '1') THE
```

COMP.CE.320 High-level Synthesis

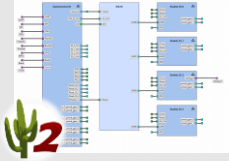
C++ to HW

”Matrix multiplication” work

COMP.CE.250 System-on-Chip Design

SoC internals, SystemVerilog

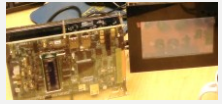
”SoC integration project”



COMP.CE.400 System Design

HW/SW co-design SystemC modeling

”Parallel streaming video encoder” work



COMP.CE.420 System-on-Chip Verification

Universal Verification Methodology

”Verification of RISC-V IO block”

PULPino

COMP.CE.510 Chip Implementation

Digital ASIC backend

”Tape-out project”

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Thank you!