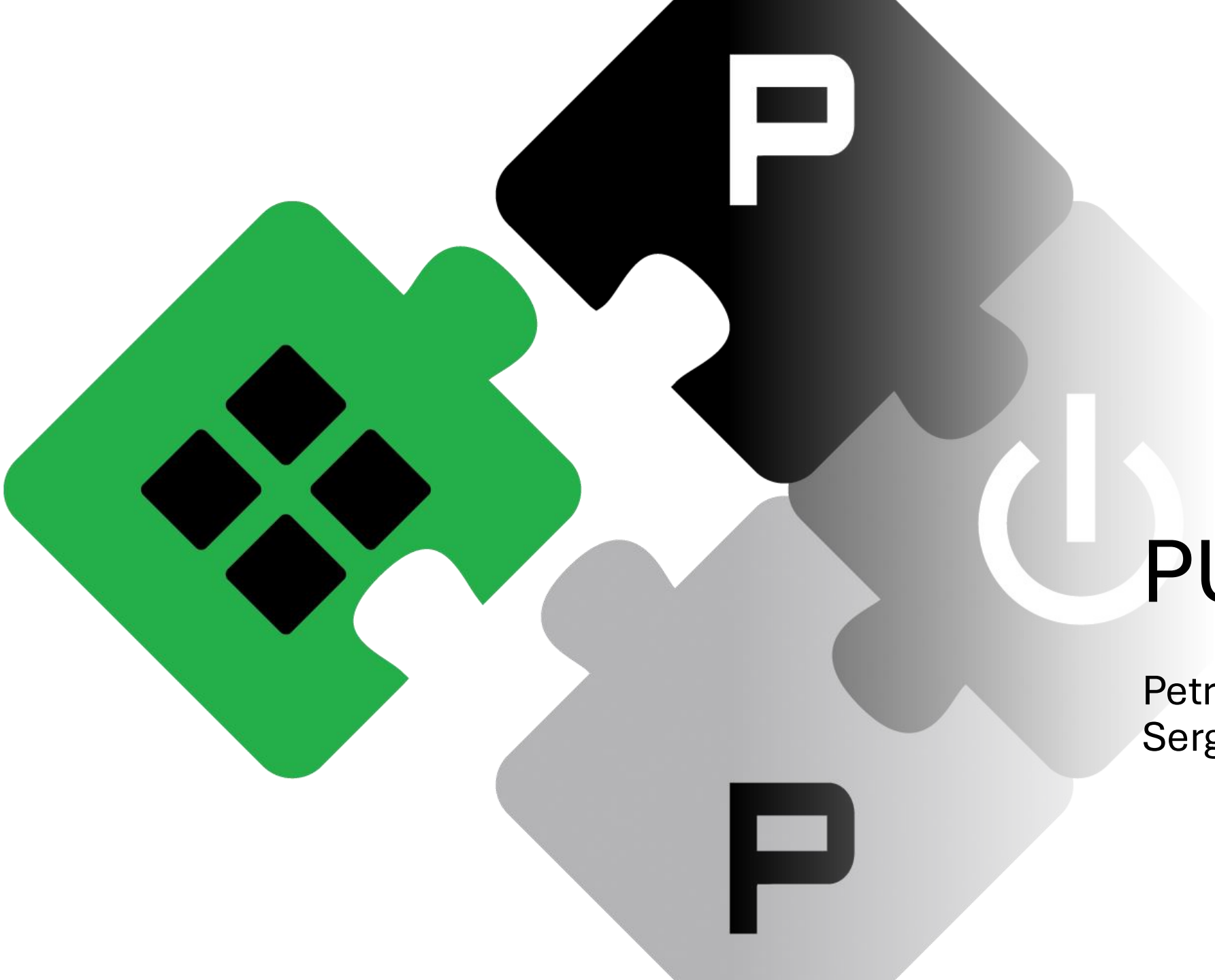


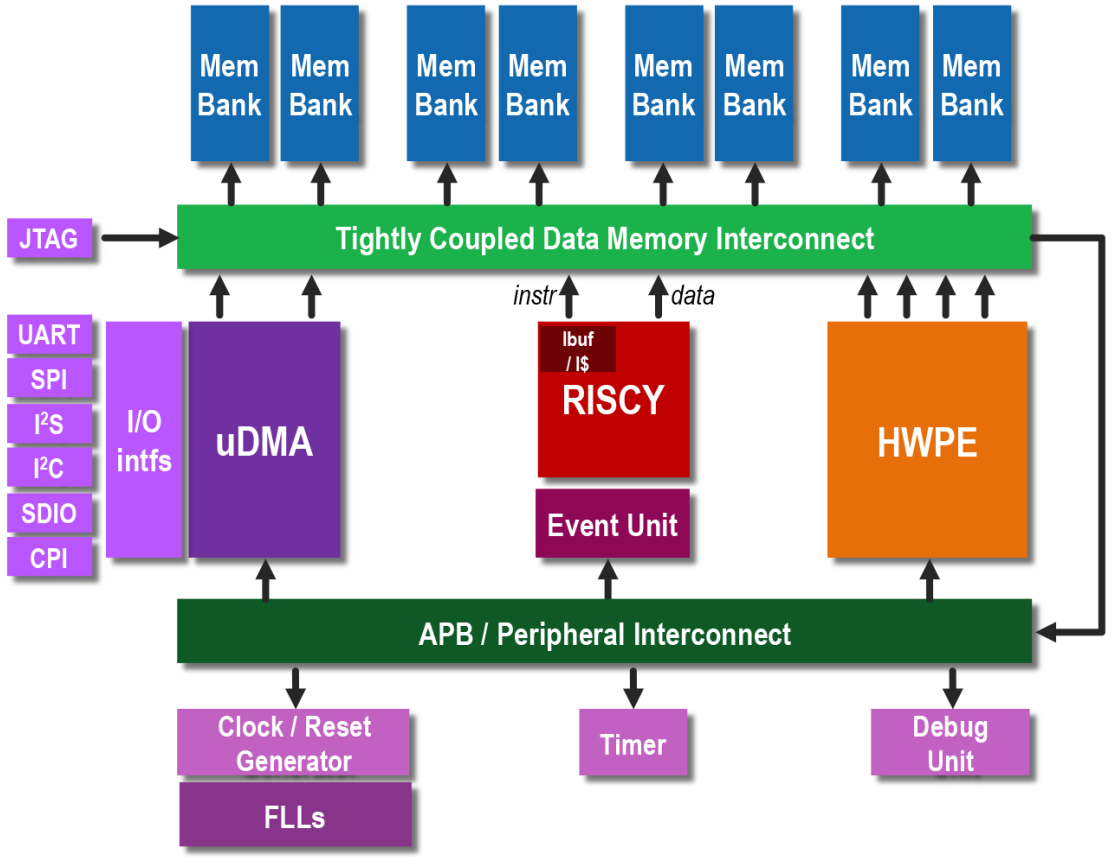
PULPissimo

Petrus Pakarinen &
Sergiu Petrut

- **What?**
  - Open-source Single-core RISC-V microcontroller System-on-Chip (SoC) platform intended for research, FPGA prototyping, and ASIC development
  - Reference microcontroller architecture used in modern PULP (Parallel Ultra-Low-Power) chips.
  - Designed for ultra-low-power embedded systems
  - Serves as the control SoC for more complex multi-core PULP chips

- **Why?**
  - Ultra-low power efficiency for embedded and signal-processing workloads
  - A complete and realistic SoC, not just a CPU core
  - Flexibility to choose between RI5CY / CV32E40P or Ibex RISC-V cores, integrate custom hardware accelerators (HWPEs) or run bare-metal, FreeRTOS, or SDK-based software

- **Who & Where?**
  - Open-Source contributors + Research Staff at ETH Zurich and the University of Bologna



How was it created?

Created with the the RI5CY core or the Ibex one as main core

Languages used listed by GitHub:

SystemVerilog, C/C++, Tcl, Python, Smarty

Supports tools like Multisim for verification

The creators also have their own tool for creating on top of the PULPissimo called Bender

License:

- SolderPad Hardware License v0.51

- Free to use, modify, manufacture, and distribute, including commercially
- Includes patent grant (terminated if you initiate patent litigation)
- Redistribution requires license, attribution, and marking modifications

Setup and Startup

- Setup is very straightforward, instructions provided in GitHub for:
  - Prerequisites
  - Simple / Full Featured Runtime
  - PulpFreeRTOS
  - How to build the RTL simultation platform
  - How to write code for the RTL platform
  - Downloading models and running them virtually / on a FPGA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