Mikko Ilmanen, Matias Aro

What is Chipyard?

- Open Source framework for agile development of Chisel-based systems-on-chip.
- Allows usage of Berkeley products to produce RISK-V SoC
- Can be used for RTL simulation, FPGA-accelerated simulation, FPGA prototyping and SoC Tape-outs.
- Used in Education
- Developed in the Berkeley Architecture Research Group in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley

How does Chipyard work?

- Chisel (based on Scala): describe digital circuits in RTL level
- Includes different tools for different flows:
  - FIRRTL and CIRCT generate (System)Verilog: RISC-V cores, accelerators, multi-level caches, peripherals, interconnects…
  - SW RTL Simulation with Verilator or Synopsys VCS
  - FPGA prototyping
  - Hammer: VLSI flow (to GDSII)
  - FireSim: FPGA-accelerated simulations
- Some tool flows easier for beginners
  - Generate RTL from pre-existing components and simulate it
- Open source and no license needed
  - If used for research, citations needed