Ibex

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What & Why?

- Ibex is a RISC-V based, open-source processor core
- It employs a 32-bit base architecture
- It is designed for embedded systems, IoT devices, and microcontrollers
- It is not a high-performance core: not built to compete with high-end desktop and mobile CPUs
- Ibex was designed with low-area, low-power, maximum security and reliability in mind
- It is available through the Apache license, and is configurable
- Desingers and engineers do not have to make a new design from scratch, but instead base their design on Ibex, and modify it to their needs

Who & where?

- Development on Ibex originally started in 2015 under the name "Zero-riscy" by the PULP team at ETH Zürich and University of Bologna.
- Since December 2018 it has been developed and maintained by lowRISC as an open source project.
- LowRISC is not-for-profit company that separated from the University of Cambridge Computer Lab in 2014. They employ a small team and describe themselves as "start-up-style".
- The company's board of directors includes people from Google and the University of Cambridge, and also independents.
- The company is a founding member of RISC-V International.

How?

- Ibex is an IP block (soft macro) written in SystemVerilog language
- Being SystemVerilog, Ibex supports pretty much all common synthesis and verification tools. Users can also add their own modifications and extensions into the block.
- Ibex is under Apache 2.0 license, which allows for free use and freedom to customize.
  - With this license, you dont have to make your own custoizations open-source
  - Apache is used to encourage commercial use
- The core itself is around 20-30k lines of code, but the git repo comes with a lot of plug-in features and documentation which adds more