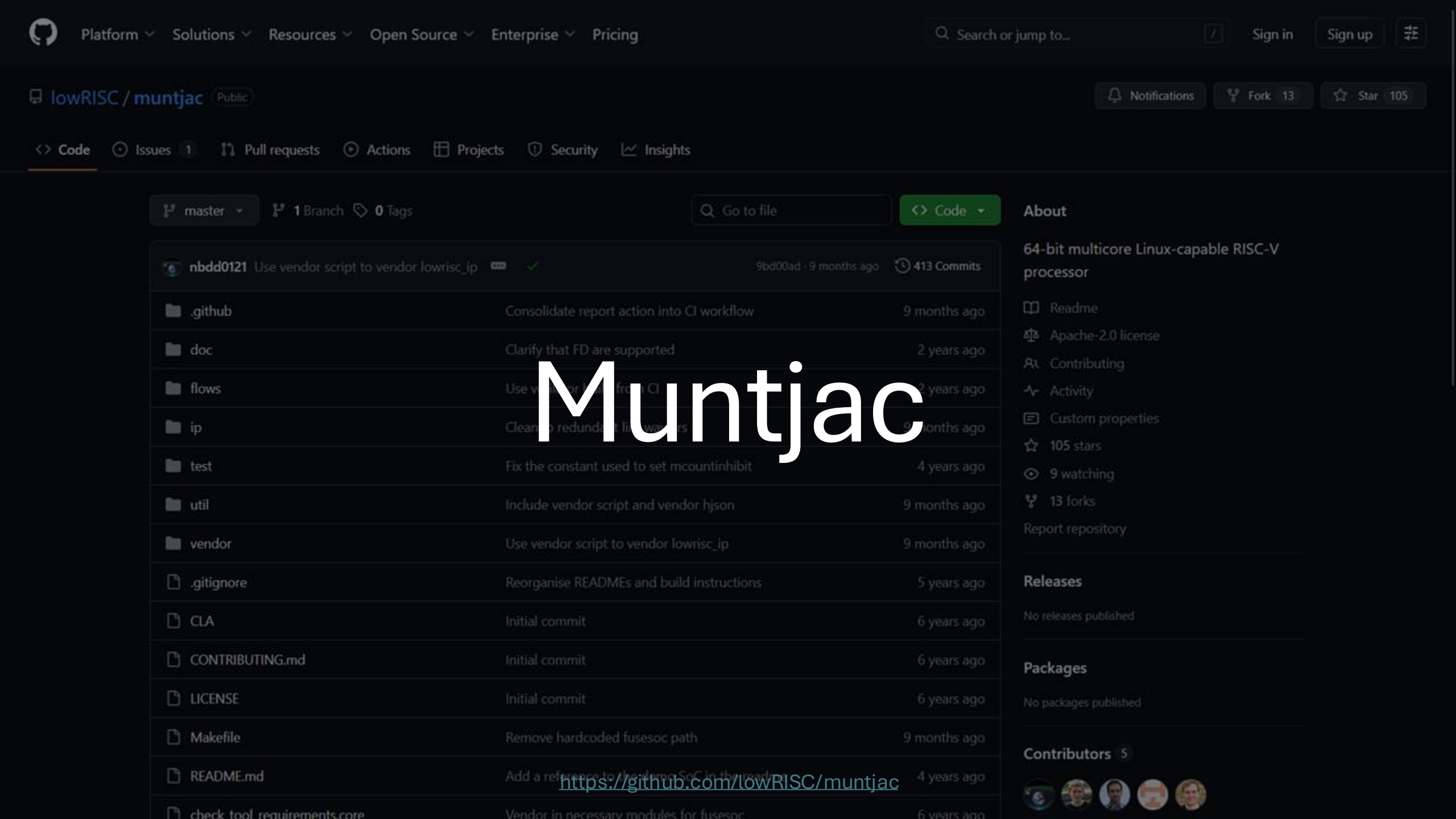


Muntjac

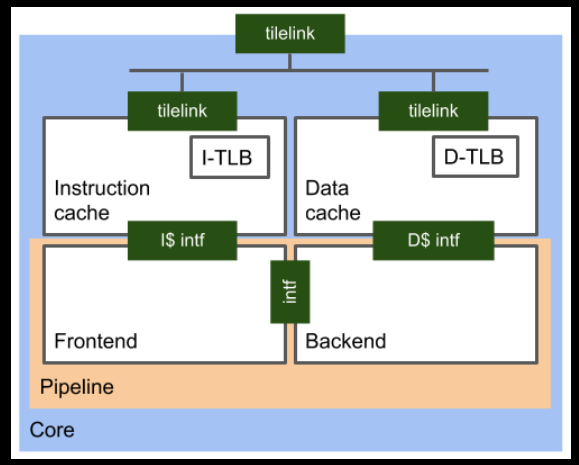
https://github.com/lowRISC/muntjac

What? What is this?

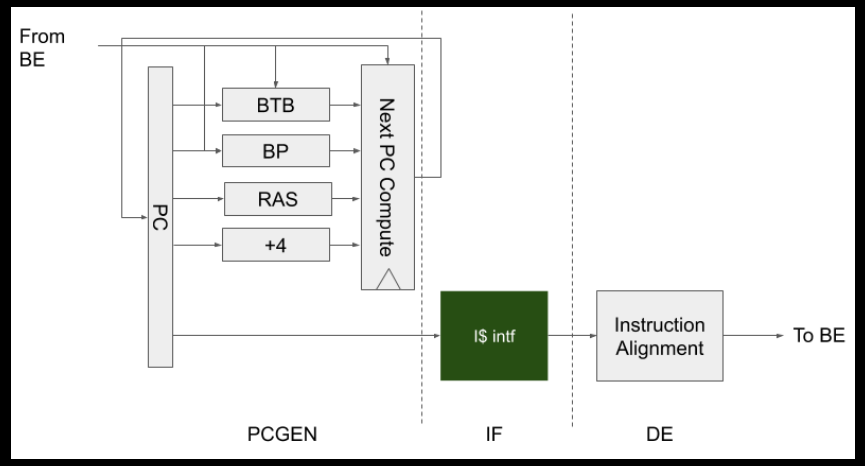
- Minimal 64-bit RISC-V multicore processor that's easy to understand, verify, and extend.
- Focuses on clean, well-tested design which others can build upon and further customise
  - SoC example also provided in another repo
- Correctness > performance
  - Baseline design for educational, academic, or real-world use.
- By lowRISC, non-profit company in Cambridge, UK
  - Works with University of Cambridge, other academic and corporate partners

Architecture

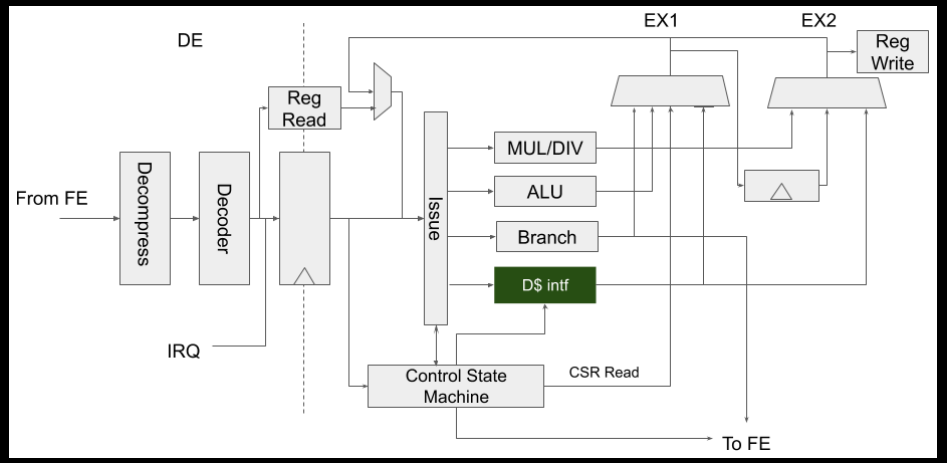
- RV64IMAC (and optional FD for floats and such)
- Supports U/S/M privilege modes and Sv39 virtual addressing
- 5-stage pipeline
- Modular architecture for easy extension and modification



Core



Front-end



Back-end

Repo

- Written in SystemVerilog
- Licensed with Apache 2.0 (quite permissive)
- Supports Verilator for simulation and Vivado for FPGA synthesis
- Also uses FuseSOC and Edalize for package management, some tests written in python, and C++ code for Verilator
  - 17.7k lines of SV, 1.7k lines of C/C++, 500 lines of python
- Has build instructions for Verilator sim
  - We tried, and failed