Chisel (Constructing Hardware in a Scala Embedded Language)

- Open-source hardware description language
  - Allows using modern high-level language (Scala) to describe digital circuits at register-transfer level while allowing advanced circuit generation.
    - Designers can write complex parameterizable circuit generators that produce synthesizable Verilog
    - Allows easy design reuse for both ASIC and FPGA digital logic designs
    - Scala is a high-level general-purpose programming language that supports object-oriented programming and functional programming.
- Is not HLS
  - Allows writing RTL code at higher level of abstraction, while still controlling exactly what is being generated
    - Combines higher abstraction and fine-grain control

```
class Add extends Module {
  val io = IO(new Bundle {
    val a = Input(UInt(8.W))
    val b = Input(UInt(8.W))
    val y = Output(UInt(8.W))
  })

  io.y := io.a + io.b
}
```

Adder written in Chisel

Creators

- Developed by Univesity of California, Berkeley
- 150 contributors on GitHub
  - Updated actively
- Part of CHIPS Alliance
  - Companies and individuals working together to develop open source CPUs, various peripherals, and complex IP blocks
  - 49 member organizations

Tools

- Circuit IR Compilers and Tools
- License with Chisel offers full controll of the software without restrictions (Apache 2.0)
- 125374 lines of code (97.6% scala, 0.9% C++, 0.4% Python)

Materials

- There are extensive tutorials on the Chisel github page.
  - These included online bootcamp, seperate github project for tutorial environment, installation guide and a book that was free to read.

- The guides were good and easy to follow
  - They started from simple hello worlds and led blinking on the fpga. The online bootcamp had connection issues.