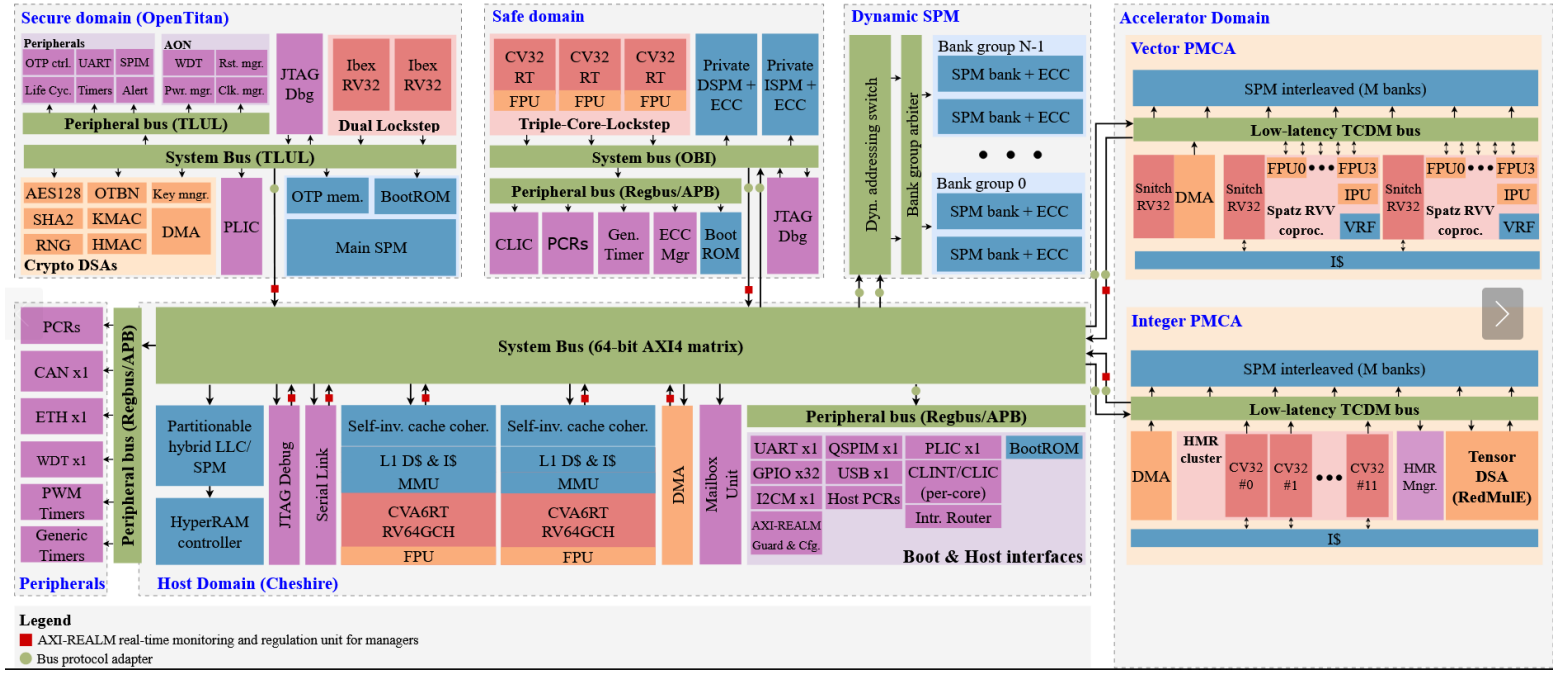
Carfield

- ETH Zurich and University of Bologna as part of PULP (Parallel Ultra Low Power) project
- Created for Mixed-Criticality Applications - Heterogeneous architecture
  - Linux capable, time-critical tasks, data encryption/decryption, robust fault recovery



- Promises ready to use FPGA flow
- HW in SystemVerilog, SW in DeviceTree Sources (Describing HW for Linux kernel coding)
- Does have ‘Getting started’ section in Github with system requirements and build instructions

  And large user manual for both architecture and software stack
- However only simulation is available open-source, synthesis and physical implementation under nonfree repository

  They will also be added to the open-source repository eventually
- Uses Cheshire (part of PULP)
- For Xilinx FPGAs
- Use under the Apache 2.0 license