Tampere University

COMP.CE.510
Chip Implementation

Lecture Starts. 14.15

Tampere University

Introduction- Chip Implementation

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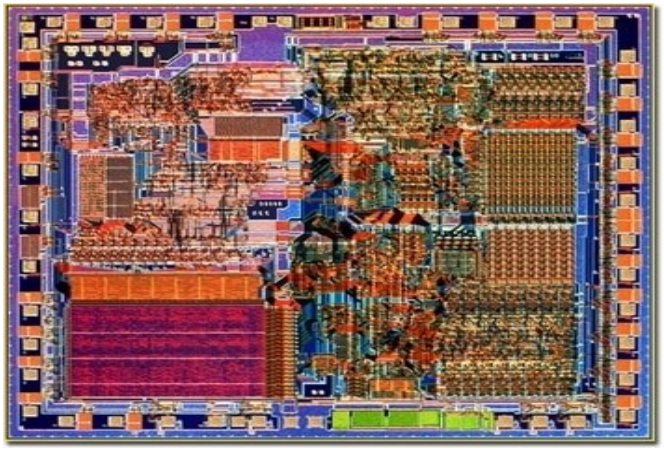
Tampere University, Finland

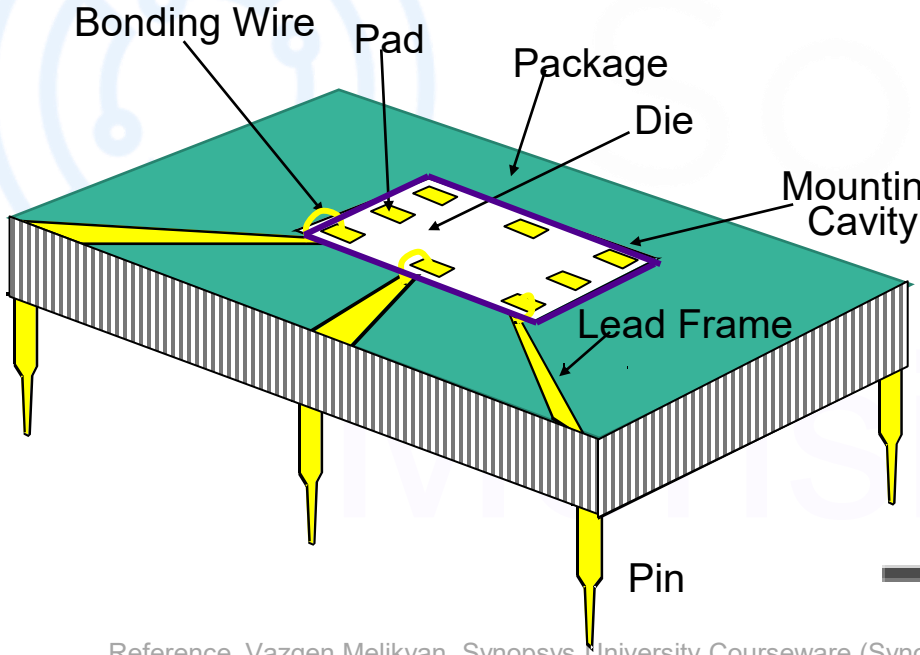
Semiconductor Chips

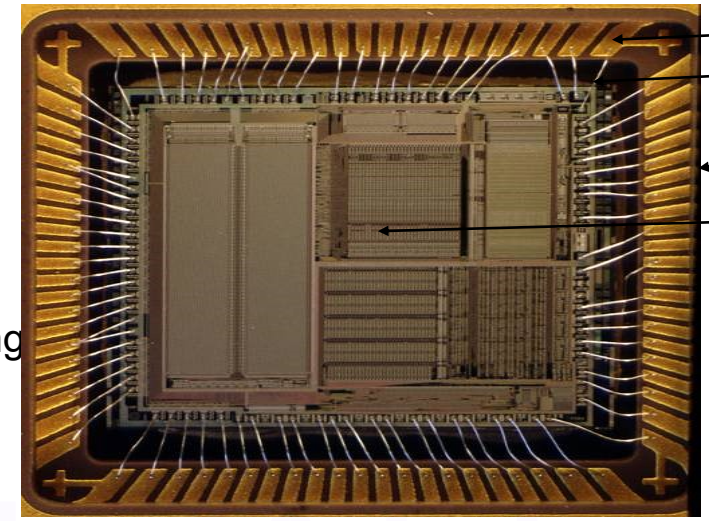
- Semiconductor chips are used everywhere:
  - Computers
  - Cellular phones
  - Tablets
  - Gaming systems
  - DVD players, TVs
  - Watches
  - Cars
  - Medical devices
  - Pacemakers and coffee pots
  - Space stations
  - Greeting cards

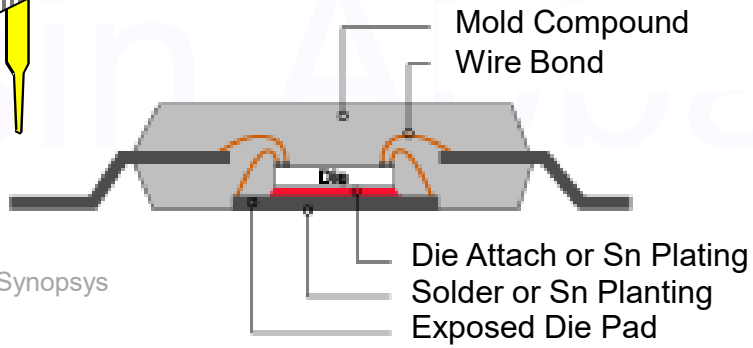
Semiconductor Chips



- Integrated circuits (IC) is a complex set of electronic components, and their interconnections etched on a chip.

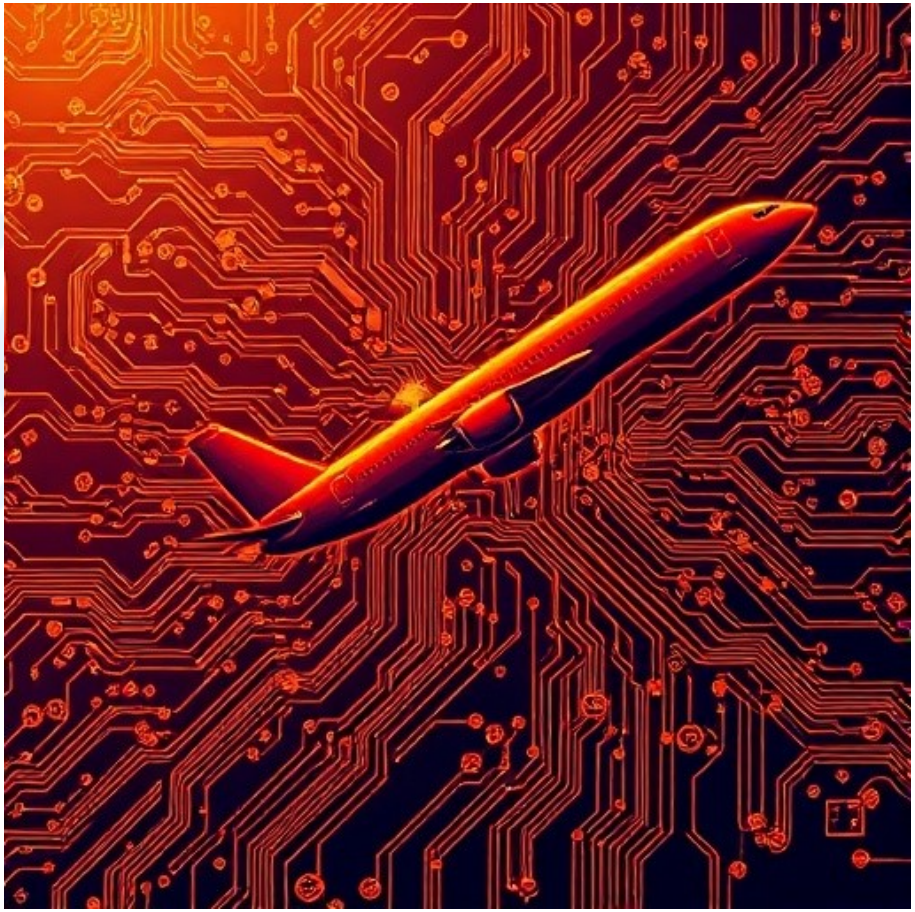






Reference. Vazgen Melikyan, Synopsys University Courseware (Synopsys confidential information)

IC Design/Chip Implementation is as easy as flying a plane……..



https://www.writecream.com/ai-generator-bing/ (Image Generated by AI)

Course Contents

- Lecture 1: Introduction- Chip Implementation
- Lecture 2: RTL-to-GDSII The Bare Minimum
  - Also Serves as LAB 1
- Lecture 3: Static Timing Analysis (STA)
- Lecture 4: Logical Synthesis
- Lecture 5: Logical Synthesis- Optimization and DFT
- Lecture 6: To Physical Domain-Floor Planning
- Lecture 7: Placement
- Lecture 8: Clock Tree Synthesis (CTS)
- Lecture 9: Routing
- Lecture 10: Chip Finishing
- Lecture 11: I/O Cells and Packaging
- Lecture 12: Low Power Design and Fabrication Process Flow

Tampere University

Lab Sessions

Teachers

- Syed Mohsin Abbas
- **Tero Lehtinen**
- Matti Käyrä
- Arto Oinonen

1. **Introduction to design flow (From 11th Sep.)**
2. **Static Timing Aanalysis**
3. **Logical Synthesis**
4. **Scan insertion + ATPG**
5. **Formal Verification**
6. **Floorplanning I**
7. **Floorplanning II**
8. **Clock Tree Synthesis**
9. **DRC & LVS**
10. **Competition**

Thursday and Friday
14.00–16.00 (TC217)

Competition (10 Points)

Given RTL, students need to run full flow RTL2GDSII - flow using it. They “compete” against a reference implementation. Points will be awarded for:

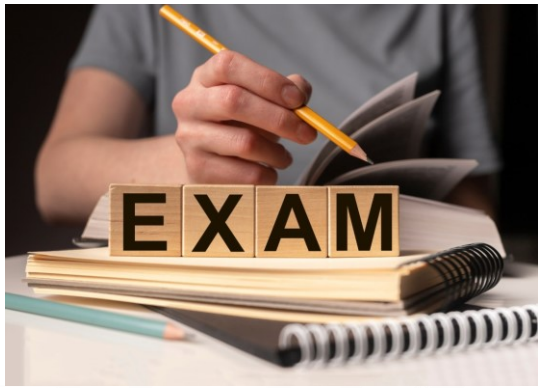
- Area
- Max clock frequency
- Total power consumption (vcd/activity file will be provided)
- Test coverage
- Flow run-time

Design will have to pass all checks: timing needs to be clean, DRC & LVS ok, formal verification ok, test coverage > 98%

Have to sign NDA

Exam and Grading

- Grading Criterion (100 Points)
  - 45 points Electronic exam (From lectures)
  - 45 points Lab Sessions
    - 5 points/Lab (Lab. 1 – 9)
  - 10 points for competition



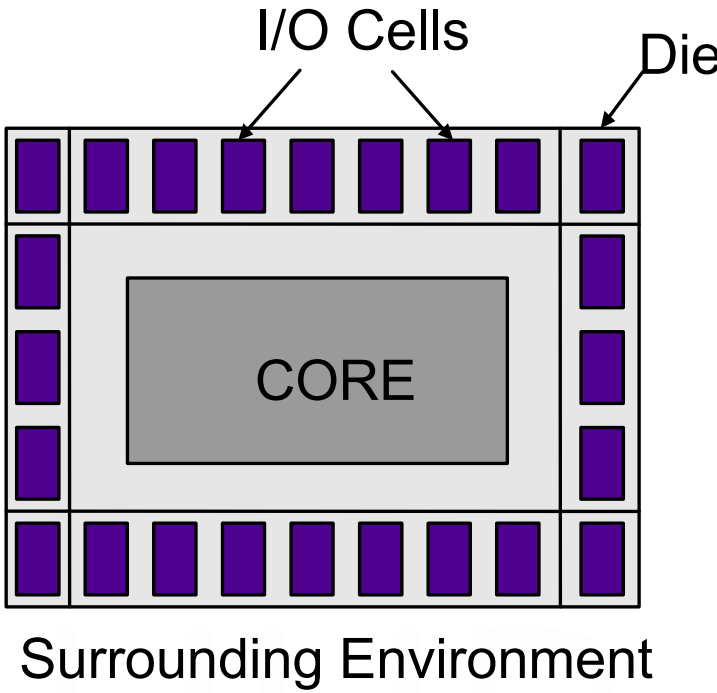
- Grades (1-5)
  - Grade 5 (90+ points)
  - Grade 4 (80+ points)
  - Grade 3 (70+ points)
  - Grade 2 (60+ points)
  - Grade 1 (50+ points)

Passing points (50)
- Atleast 6 labs (30 points)
- Atleast 20+ marks in Exam.

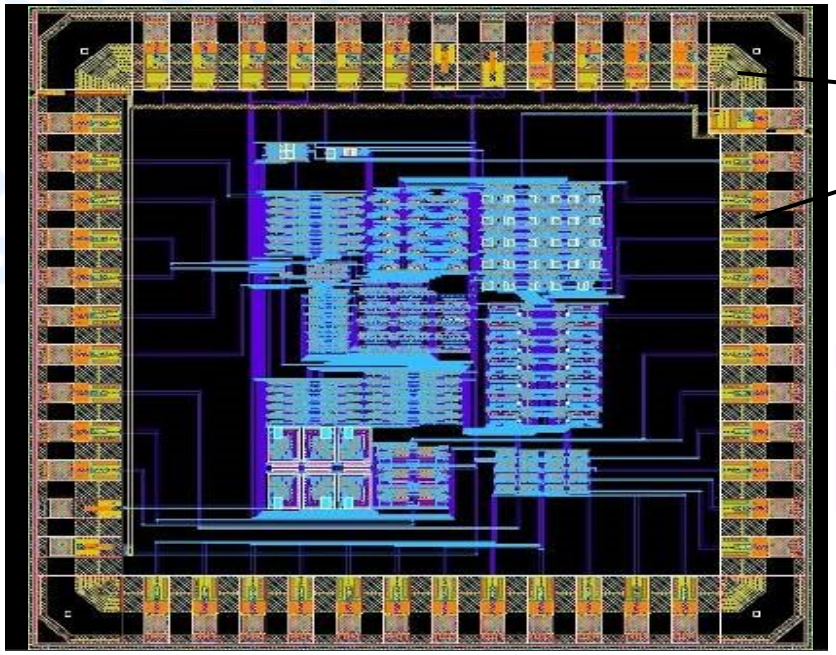
Mattermost registration:
https://mattermost.tut.fi/signup_user_complete/?id=yf3x7e9xo3f4jy5um9pyr9a35y
Course channel: https://mattermost.tut.fi/studentsetstaff/channels/compce510

Image sources. https://k8school.com/importance-of-exams/
Image sources. https://www.compute.dtu.dk/news/chip-design

IC Structure: Core, IO Cells

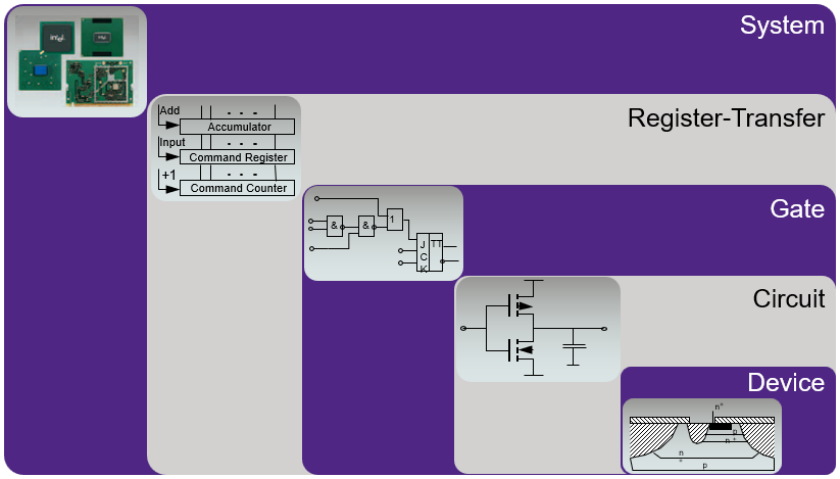


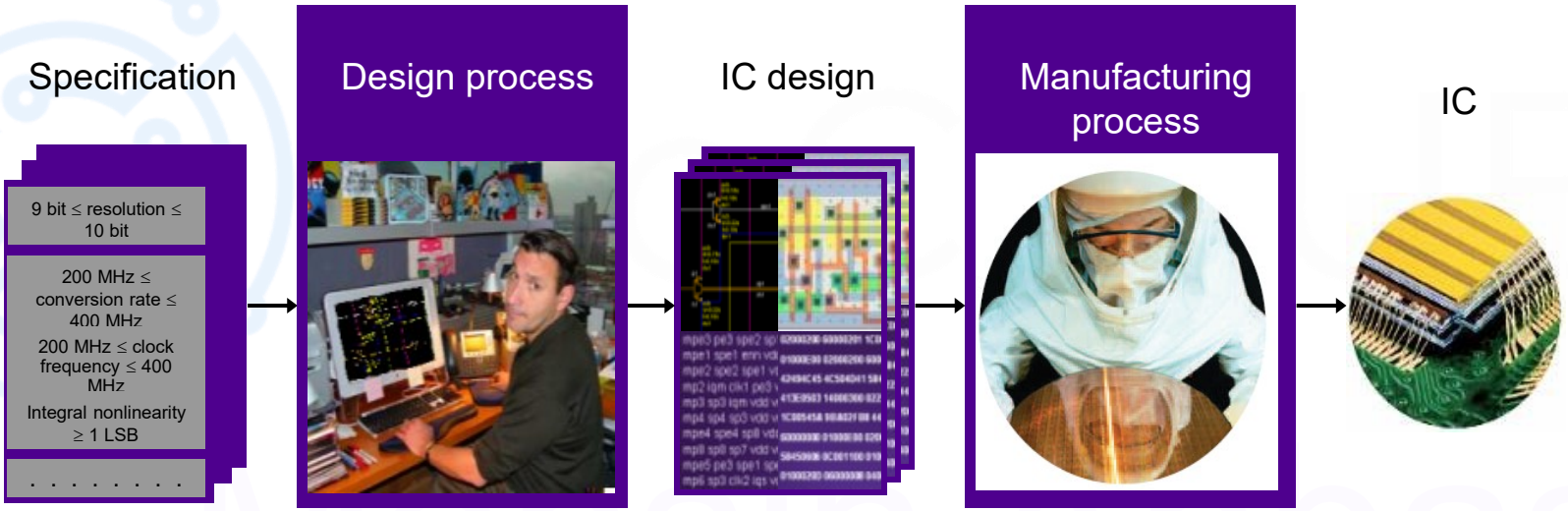
Core - provides basic functionality of IC



I/O Cell – provides accordance between the Core and surrounding environment (voltage levels, signal transfer velocity, resistances, etc).

Phases of IC Design



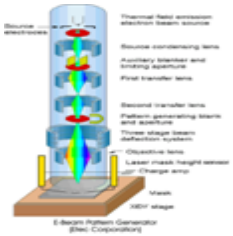


Design process is the process of getting IC design from specification

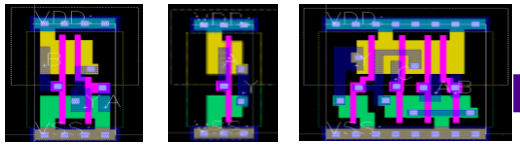
Digital Design Flow

Design Rules

Process



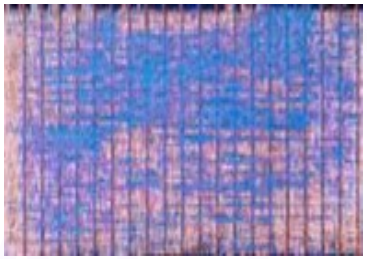
Cell Library



```
process begin
  wait until not
    CLOCK'stable
    and CLOCK=1;
  if(ENABLE='1') then
    TOGGLE<= not
  TOGGLE;
  end if;
end process;
```

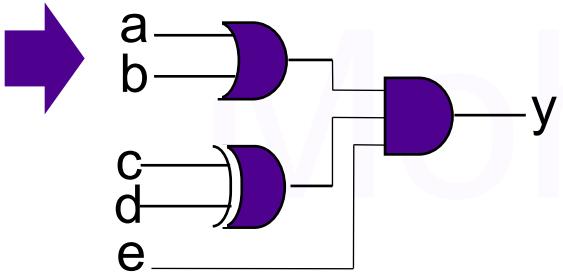
RTL / Logic

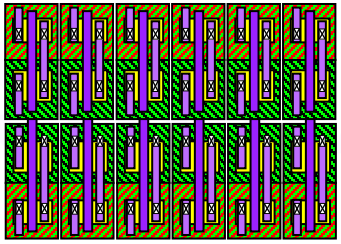
EDA Tools



Design

Y=(a+b)&(c⊕d)&e



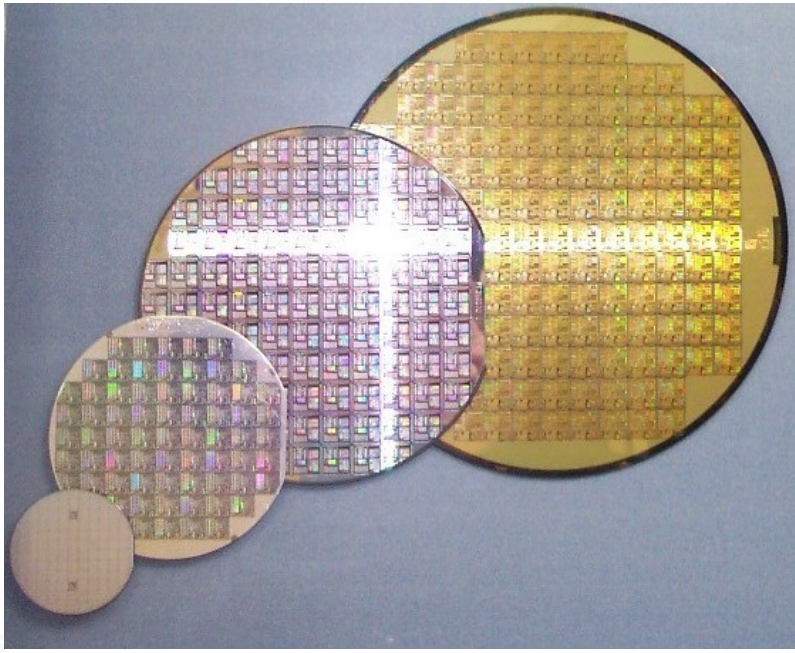


Design.gds

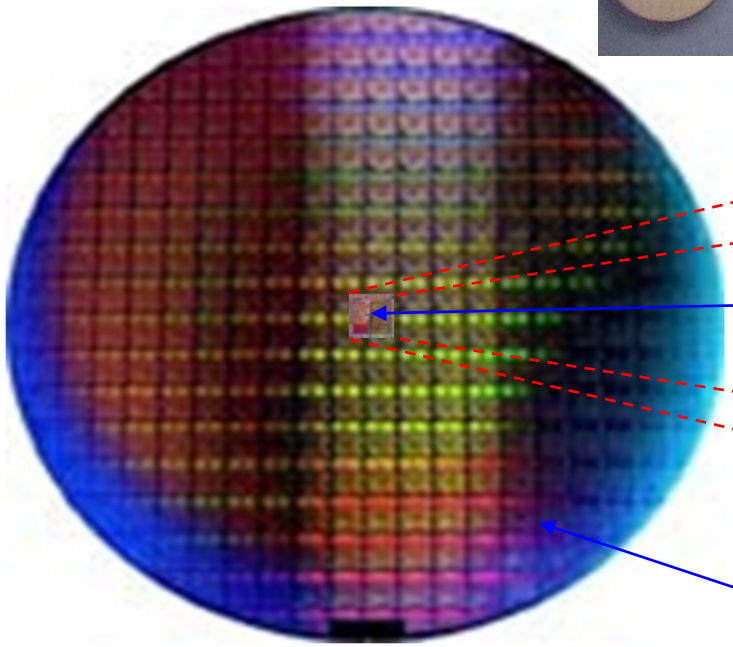
```
02000200 60000201 1C000300
02000600 .........`.... 000000

01000E00 02000200 60002500
01000E00 .....%.`..... 000010

42494C45 4C504D41 58450602
12002500 .%....EXAMPLELIB 00002
```

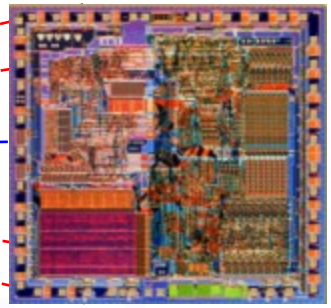
Wafer and Die

- ICs are fabricated on circular slices of silicon called wafers.
  - Wafer contains various identical dies.



Side view of a Wafer





Die

Top view of a die

Wafer

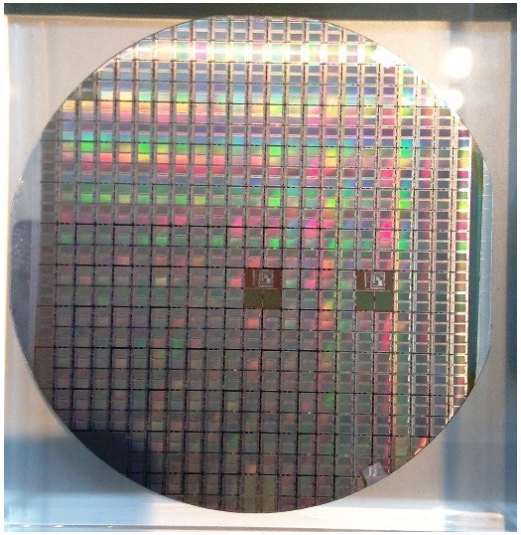
Wafer

- Wafer is cut from metal-cast of single crystal silicon




Wafer

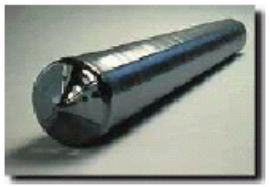
- Wafer is cut from metal-cast of single crystal silicon

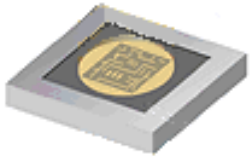


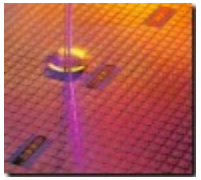
IC Fabrication- Simplified

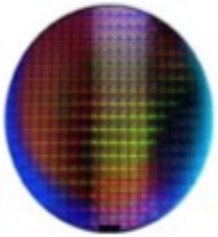
The series of steps used to create integrated circuits is called the semiconductor fabrication process.

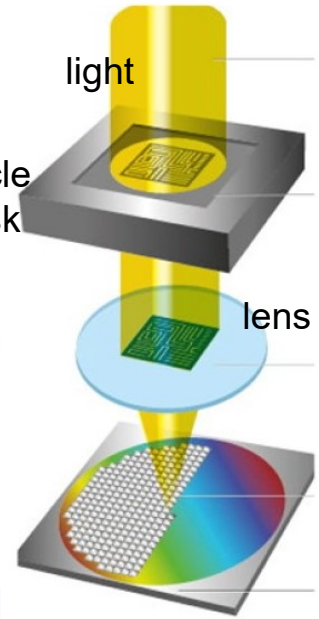
1. Growing of a giant crystal of silicon
2. Slicing it up into round wafers and polish them.
3. Coating of a wafer with a photographic chemical that hardens when exposed to light (Photoresist Coating)
4. Taking a picture of a pattern to embed in the silicon (Photolithography).
5. Shrinking of the picture and shining a light through it (Exposure)
6. Dipping of the wafer in acid (Etching)
7. Repetition of steps 3 - 6 many times, producing layers of patterns etched into the wafer (Metal layer deposition)
8. Slicing up the wafer into many rectangle chips.
9. IC Packaging
10. IC Testing
11. PCB Mounting



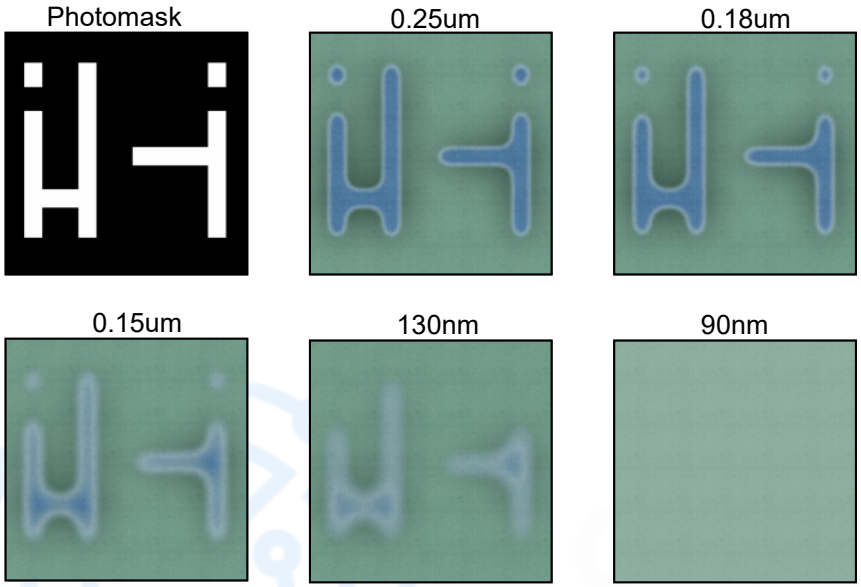








Challenges in IC Fabrication



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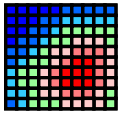
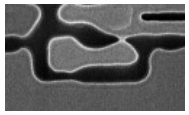
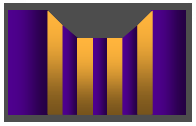


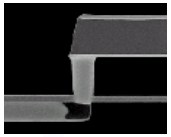
Tech. deviations



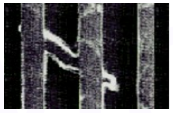
Lithography



Interconnects deformation



Interlayer connections



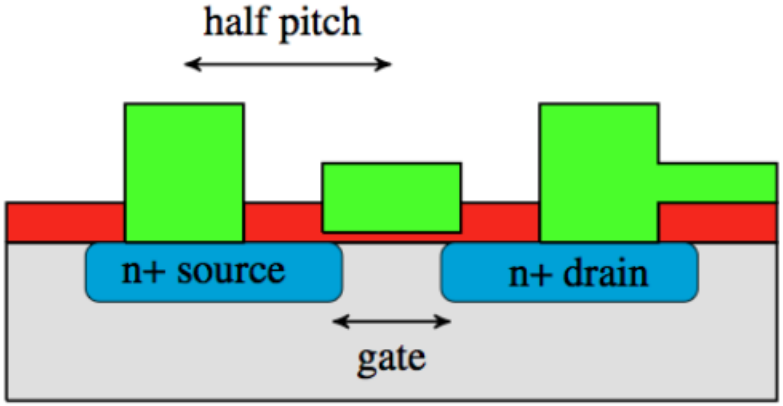
Short connections

20um, 10um, 5um, 2um, 1um, 0.5um, 0.25um, 0.18um, 0.13um, 90nm, 65nm, 45nm, 32nm, 28nm, 22nm, 20nm, 14nm, 7nm, 5nm, 3nm …

Largest IC Foundries

TSMC	Taiwan Semiconductor Manufacturing Company
GF	Global Foundries
UMC	United Microelectronics Corporation
Samsung	Samsung
SMIC	Semiconductor Manufacturing International Corporation
TowerJazz	Tower Semiconductor
ELMOS	Elmos Semiconductor AG
XFAB	Mixed-Signal Foundry Expert

Process/Technology Nodes

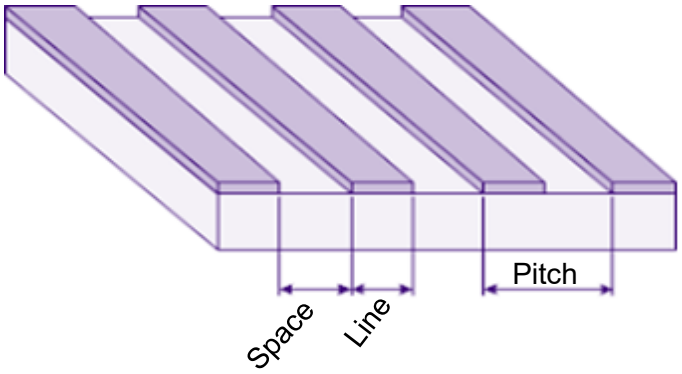


Technology node - concerns to a specific semiconductor process and its design rules.

- The smaller technology node means the smaller feature size.
  - Gate length and metal1(M1) half-pitch.
- Recent technology nodes such as 22nm, 16nm, 14nm, and 10nm refer to a specific generation of chips and does not correspond to any geometric parameter.

For example, in 2005, the node on an Intel microprocessor was 65nm, the gate width was 32nm, but the half pitch was 105nm.

Process/Technology Nodes



Example processes. Each has its own design rules.

- TSMC 22nm G Logic 1.0V/3.3V
- SMIC 45nm LL Logic 1.2V/3.3V
- SMIC 45nm LV Logic 1.0V/3.3V
- Samsung 32nm LP Logic 1.2V/3.3V
- UMC 32nm LL Logic 1.2V/2.5V
- Samsung 14nm LP Logic 0.8V/1.5V
- UMC 14nm LL Logic 0.8V/1.8V

G – generic
LL – low leakage
LV – low voltage
LP – low power

Design Rules - Rules constructed to ensure that design works even when small fabrication errors occur

Process Nodes

Planar
- 500 nm
- 350 nm
- 250 nm
- 180 nm
- 130 nm
- 90 nm
- 65 nm
- 45 nm
- 32 nm
- 28 nm
- 22 nm

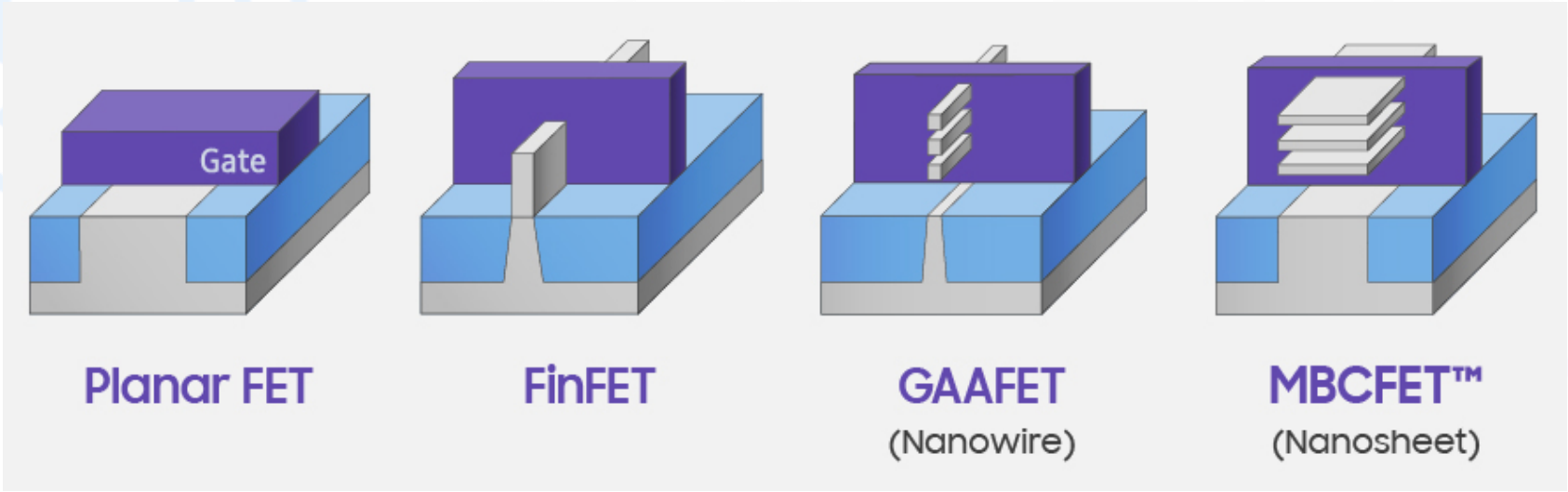
FinFET
- 16 nm
- 12 nm
- 10 nm
- 7nm
- 5nm
- 3nm

FinFET Advantages

- Better control over the channel
- Suppressed short-channel effects
- Lower static leakage current
- Faster switching speed
- Low power consumption

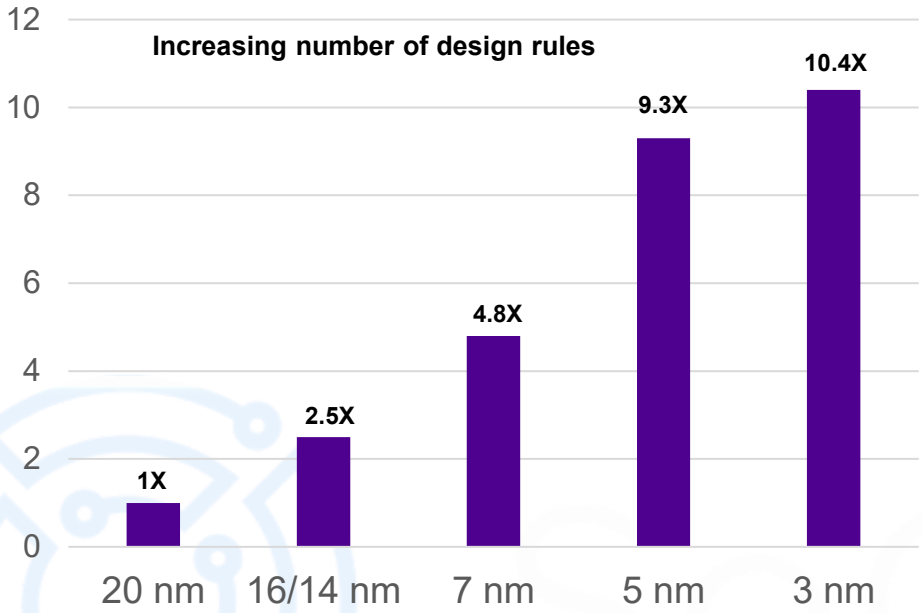
< 22 nm

< 3 nm

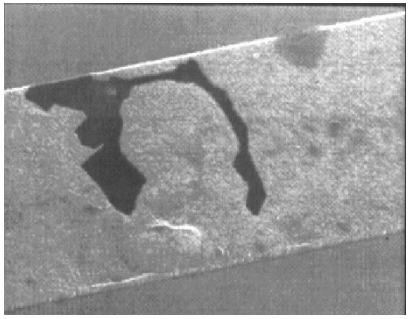


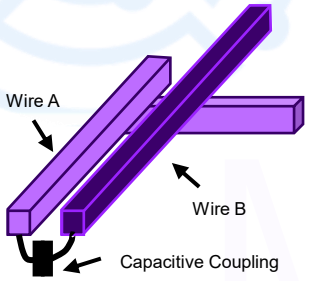
From https://www.anandtech.com/show/16041/where-are-my-gaafets-tsmc-to-stay-with-finfet-for-3nm

IC Design Challenges



Break





Signal integrity

550mln tr.
3.4GHz

54bln tr.
3.4GHz

Uncertainties
Tech. deviations
Increase in the number of Design rules

250mln tr.
2.2GHz

Power consumption
Lithography

42mln tr
1.4GHz

Signal Integrity

7.5 Million Transistors.

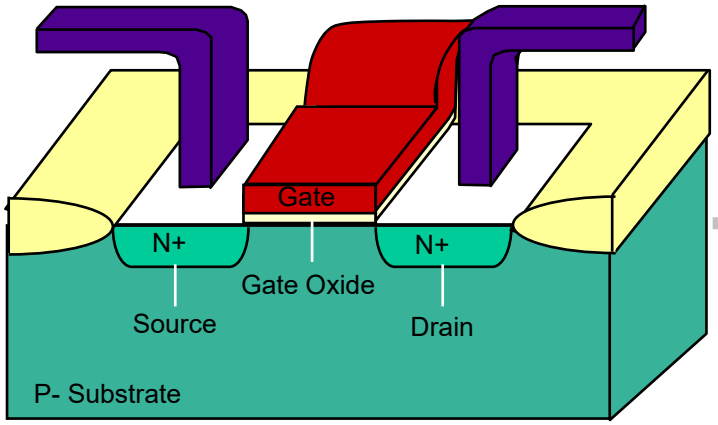
Performance
Interlayer connections

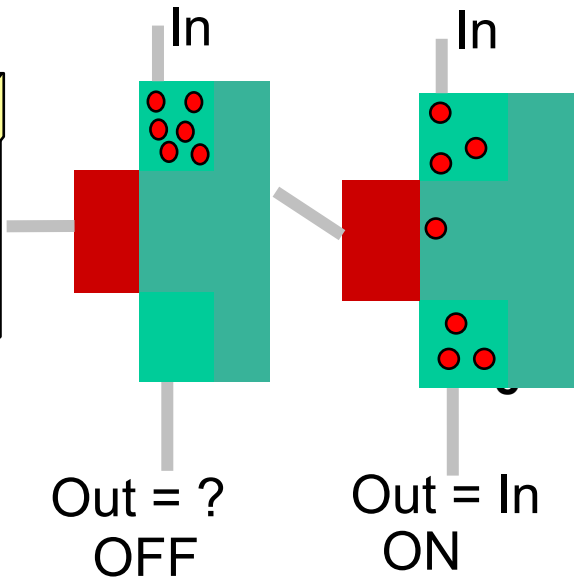
7.5mln tr.
300MHz

Performance, area

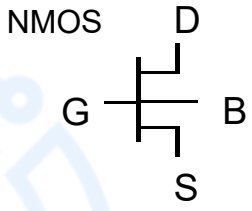
20um, 10um, 5um, 2um, 1um, 0.5um, 0.25um, 0.18um, 0.13um, 90nm, 65nm, 45nm, 32nm, 28nm, 22nm, 20nm, 14nm, 7nm, 5nm , 3nm

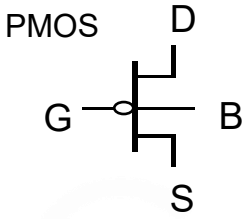
Basic Element of IC

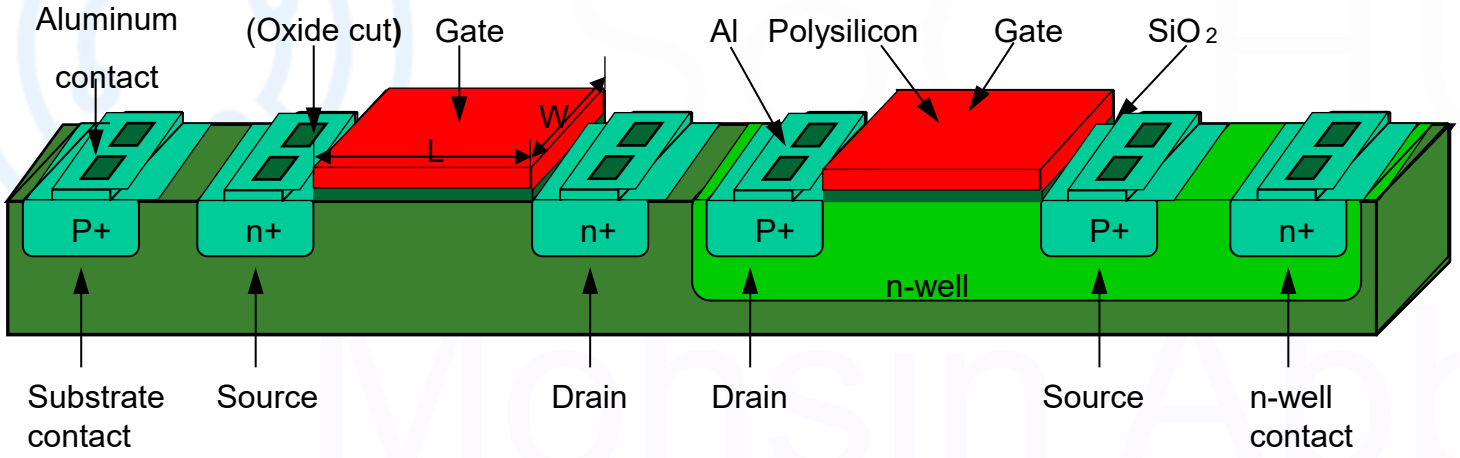


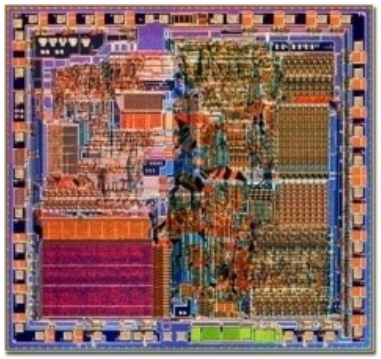


CMOS/MOS Transistor is a switch



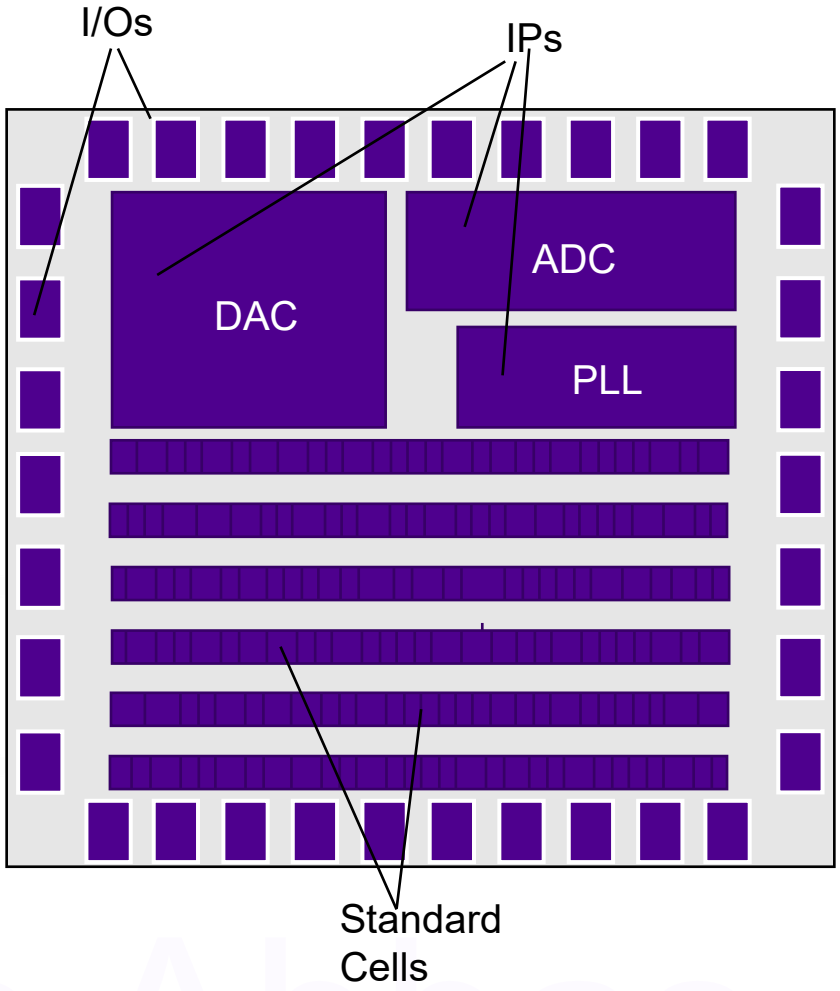






For contemporary technologies, up to a dozen of billions switches on a single chip

IC Components



Digital Standard Cells

Basic cells performing simplest functions (e.g. AND, OR, etc.) or more complex functions (Multiplexers, Latches, Flip-Flops, etc.) used as building blocks for large digital circuits

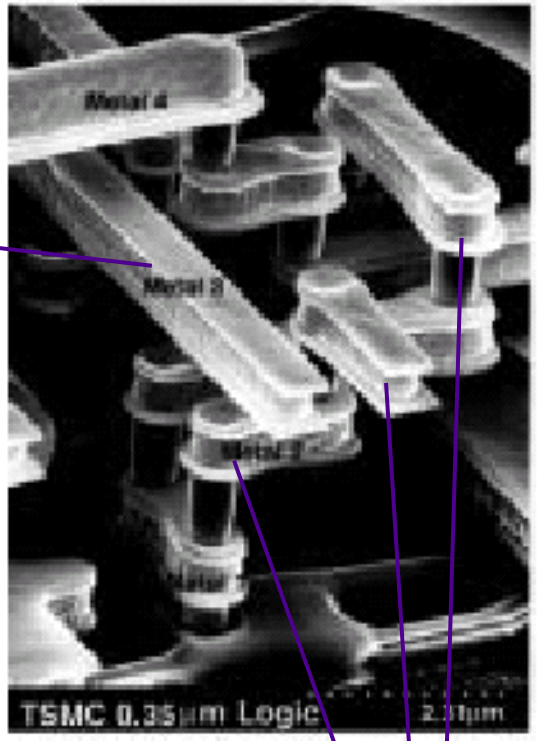
Input/Output (I/O) Cells

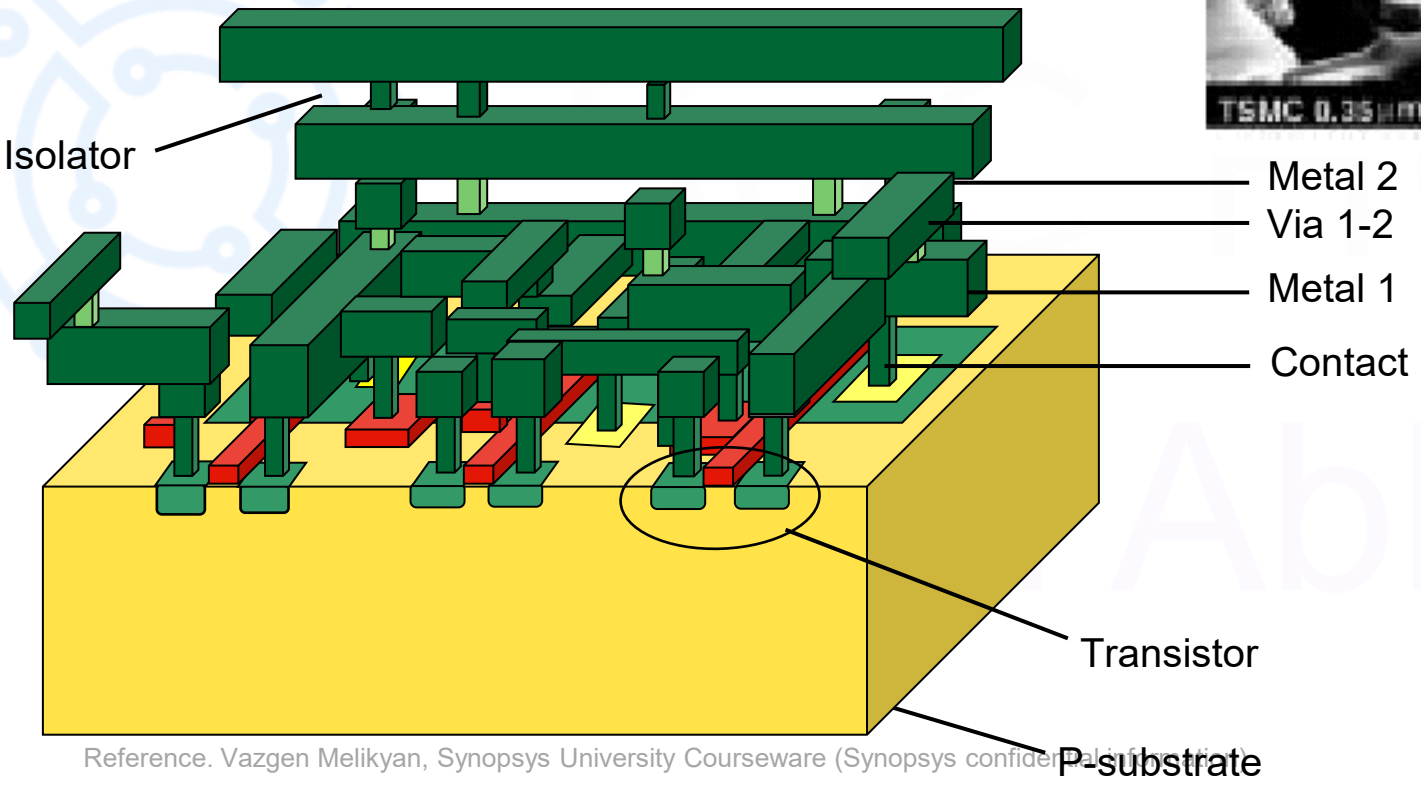
Implement the connection between IC inner circuitry and external environment (PCB)

Intellectual Property (IP) Blocks

Large blocks performing completed functions (DAC, ADC, PLL, etc), used in large designs

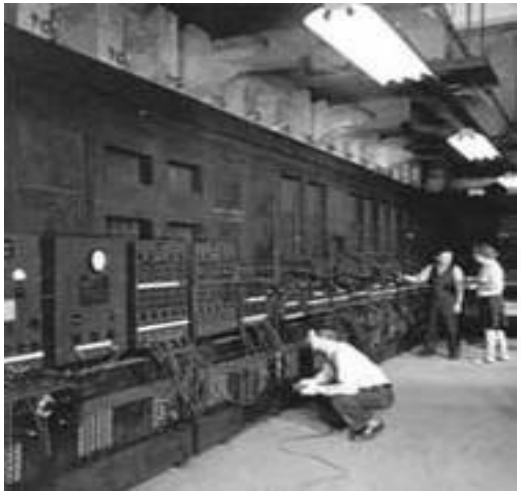
IC as a Multi Layer Structure





History and Evolution of The IC Industry

The first electronic “ENIAC” computer



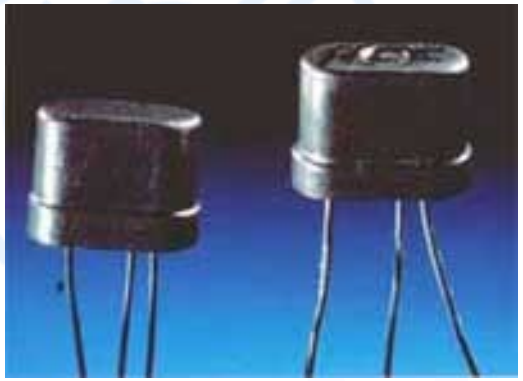
Vacuum tube

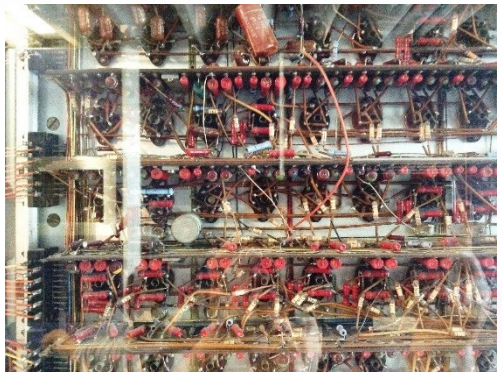
1946. The first electronic computers were created which operated by vacuum lamps

History and Evolution of The IC Industry (Transistor Computers)

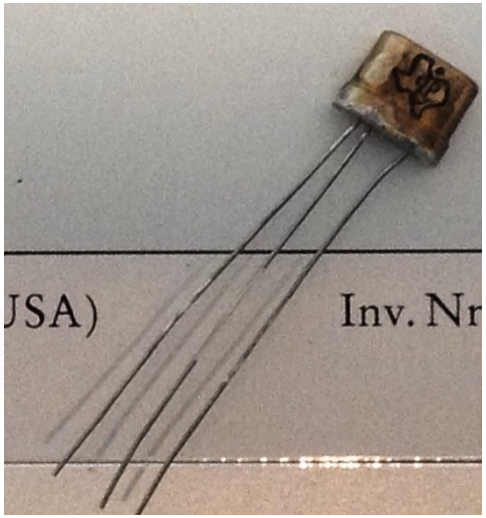
- 1948. The first transistor was created in Bell Labs

- 1954. The first fully transistor computer was developed.



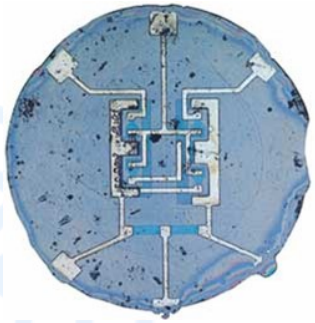


A block of fully transistor computer

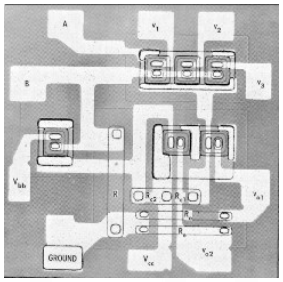


The “Birth” of an IC

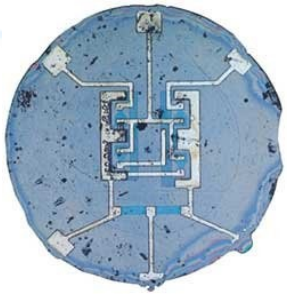
1959. The first integrated circuit was created



The first commercial IC which in 1959 was developed by the British architecture Robert Noyce and manufactured by “Texas Instruments”



3-input Gate, which in 1966 was manufactured by Motorola

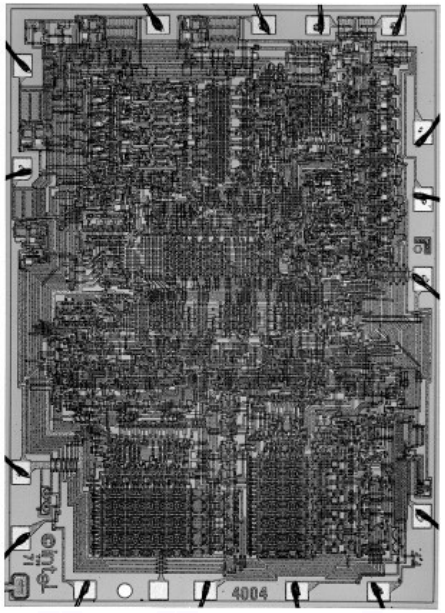


1958: Robert Noyce

1959: Jack Kilby

IC Based Computers

1971. The first microprocessor was created



Intel 4004 Microprocessor

- Developed in 1971
- Contained 1000 transistors
- 1 MHz operation

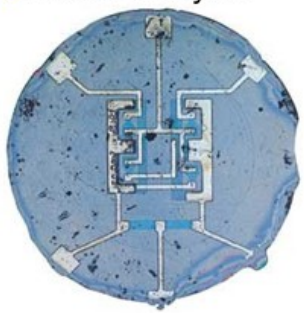
1983. Apple created the first PC

Reference. Vazgen Melikyan, Synopsys University Courseware
(Synopsys confidential information)

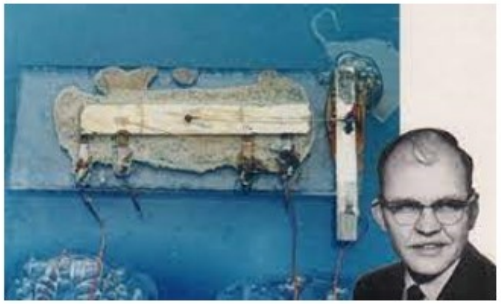
Evolution of Integrated Circuits

First integrated circuits

1958: Robert Noyce



1959: Jack Kilby



Only 66 years

- **Today's integrated circuits**

Google TPUv6

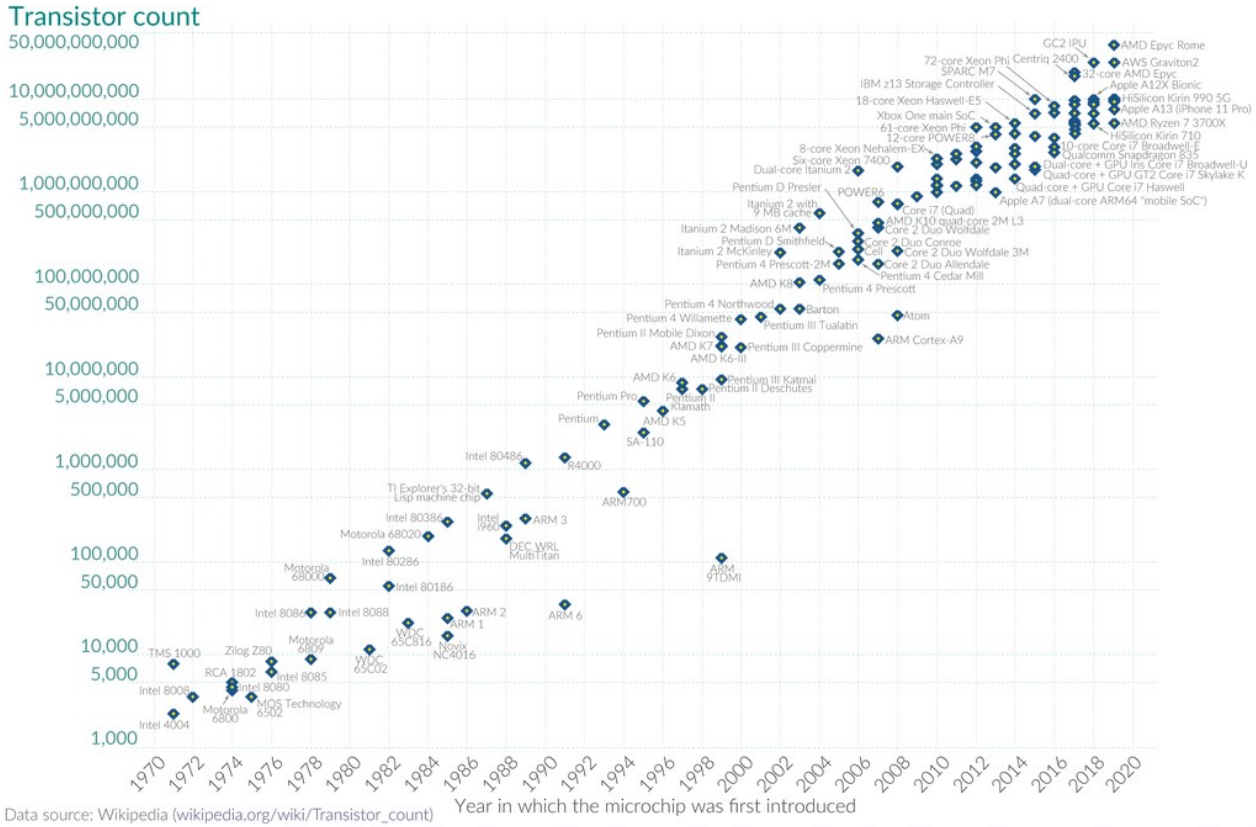
Qualcomm Snapdragon Gen 3

Huawei Kirin 9000e

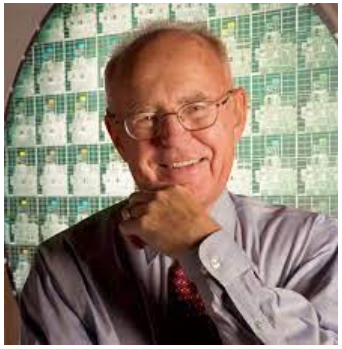
ARM Cortex-X5

Exact Prediction of IC Evolution

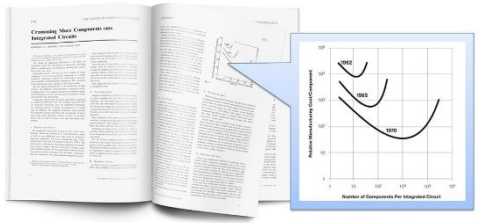
Moore's Law



Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

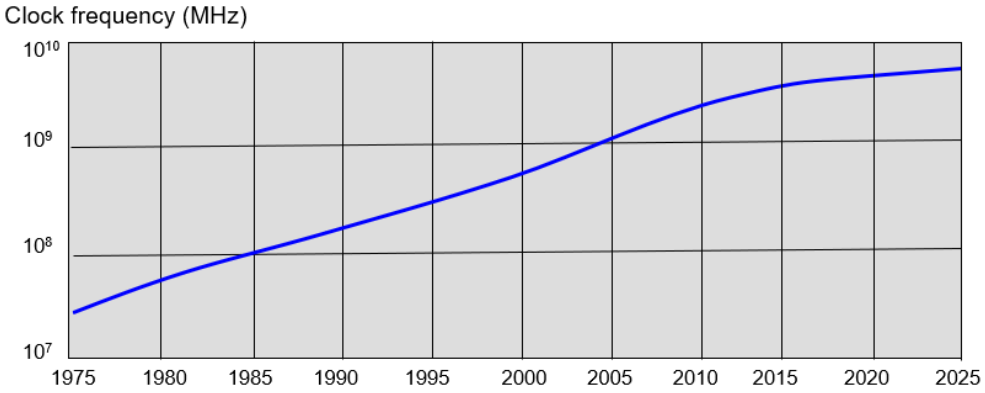


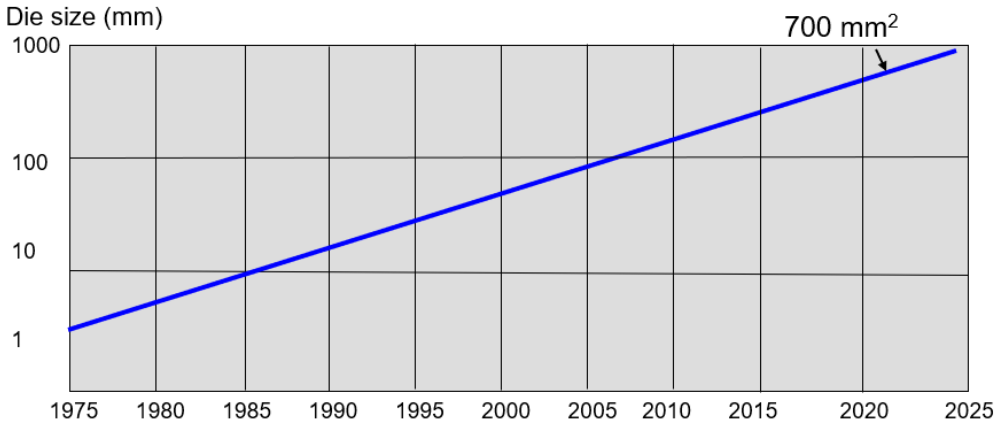
1965. The number of transistors in ICs will double every 18 months



History and Evolution of ICs

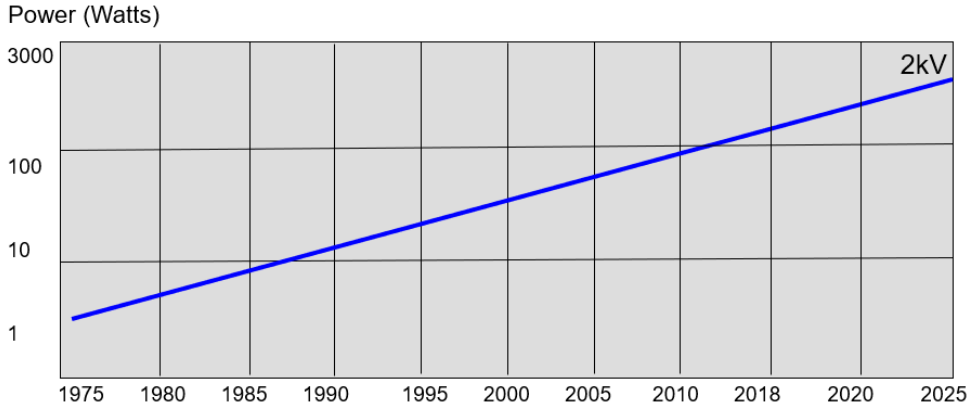
Clock frequency doubles every 2 years





Die size grows by 14% every year

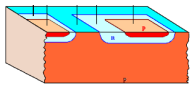
Powers increase about ten times every 3 years



Reference. Vazgen Melikyan, Synopsys University Courseware
(Synopsys confidential information)

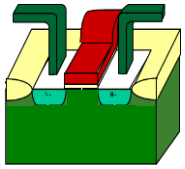
IC Scaling

- Reduction of transistor size ~10000 times
- Change of transistor type 4 times



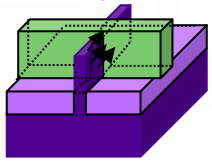
Bipolar

Less power comsuming



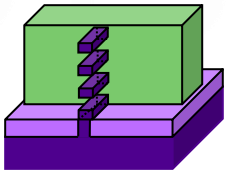
MOS

Less leakage current



FinFET

Less leakage current



GAA

20um … 2um … 14nm … 2nm

IC Scaling

Trillion transistors
10^{12}

Google TPUv6

Intel Pentium 3

First IC

3 transistors ⋯ 27 million transistors ⋯ 108 billion transistors

Increase of Specific Power Consumption

- Increase 300 times

Google TPUv6

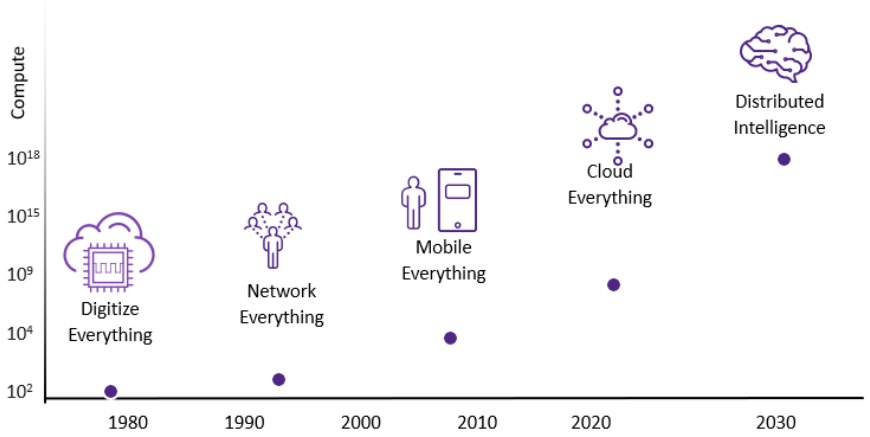
Intel Pentium 3

First IC

~1W/cm² … ~8W/cm² …

Google TPU (Tensor Processing Units)

Era of Innovations



100B
Intelligent Connected Devices

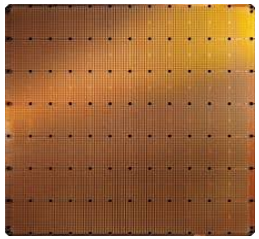
World to generate
175 Zettabytes
of data by 2025

Computing power

GTX 580
1.6 TeraFLOPS / 512 CUDA cores

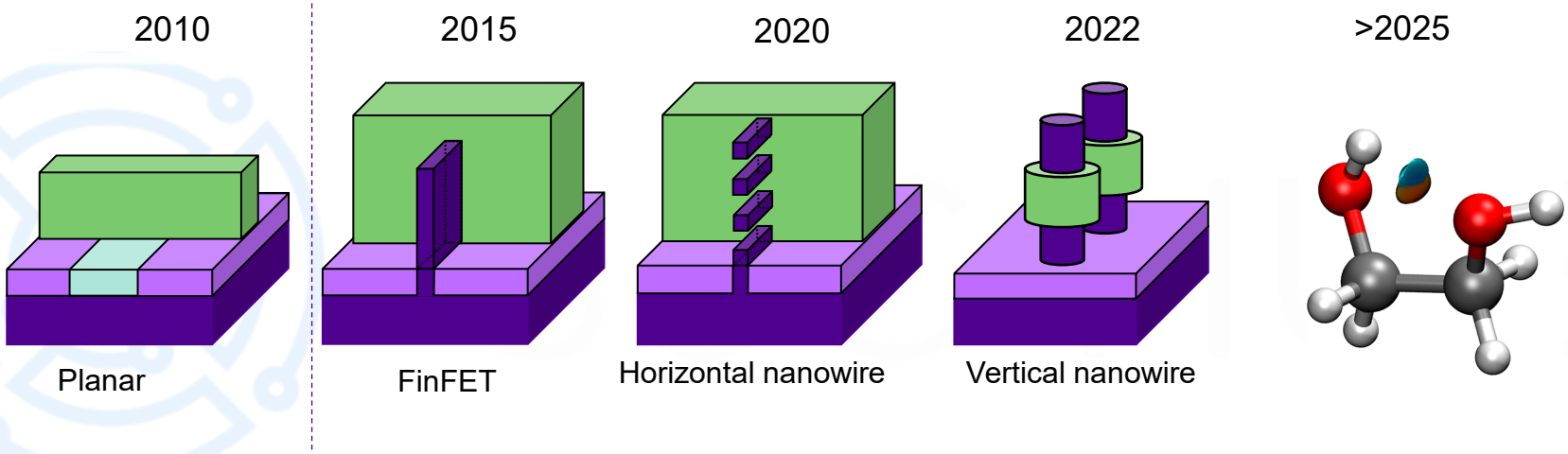
Cloud TPU v4 Pod
> 1 ExaFLOPS

WSE-2
850,000
AI-optimized cores

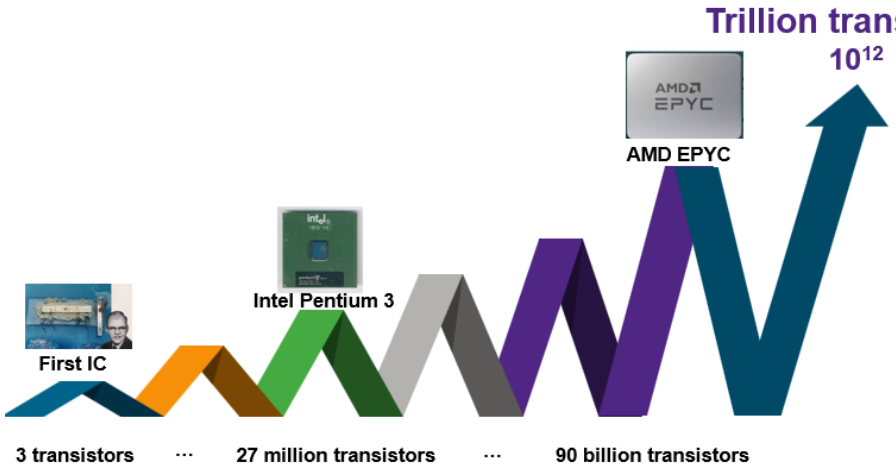


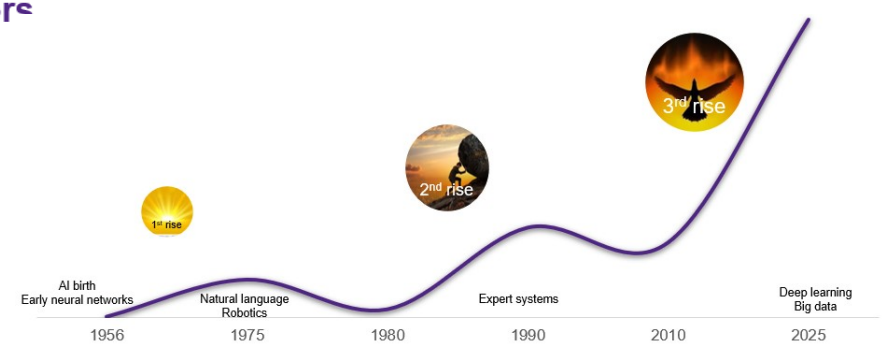
2010 2020 2025

New Era: Further Scaling



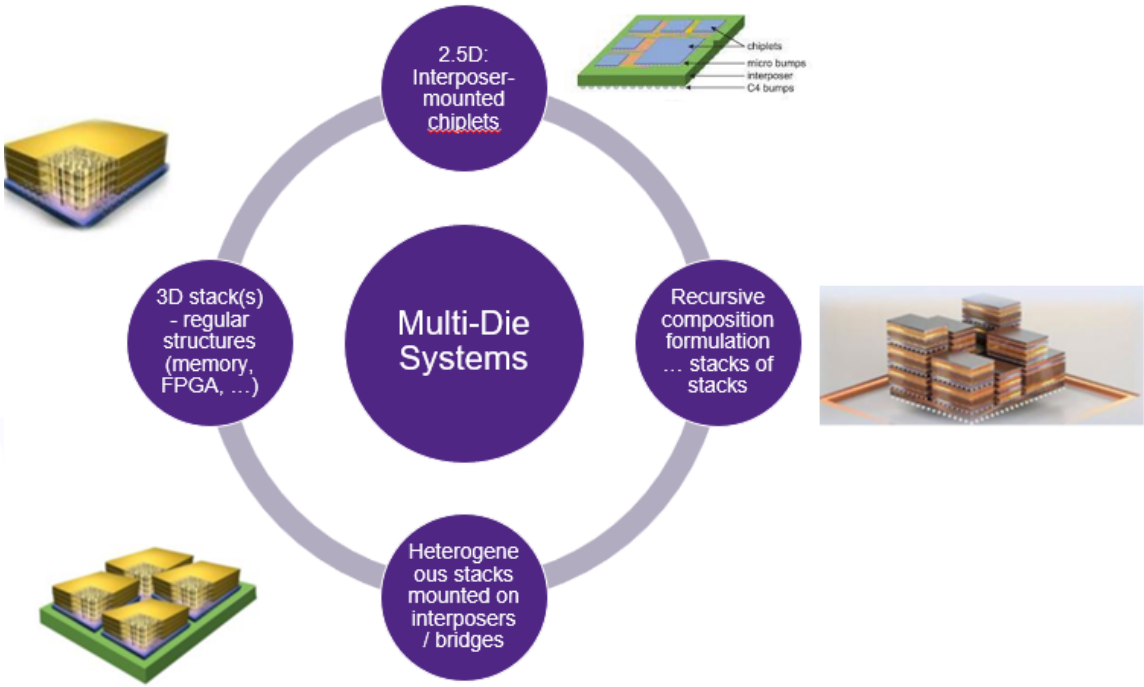
New Era: Further Scaling





Intensive Use of AI

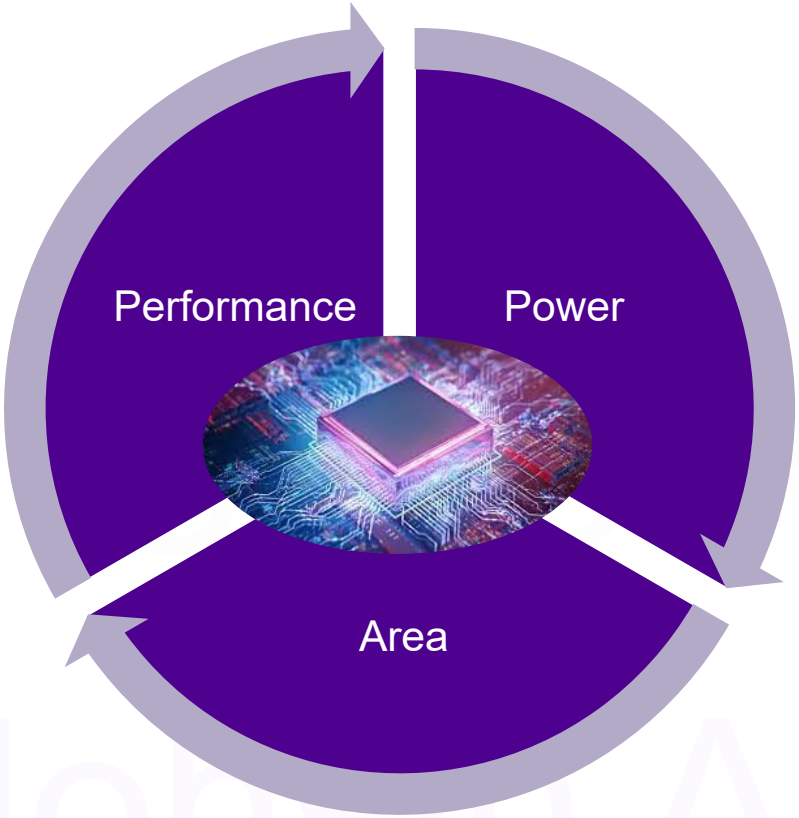
Transition from Monolithic to Multi-Die Systems



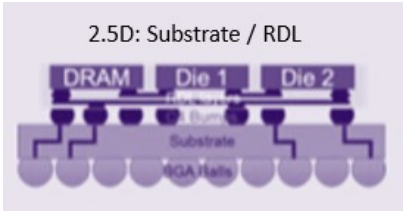
Semiconductor Industry Association (SIA) Roadmap

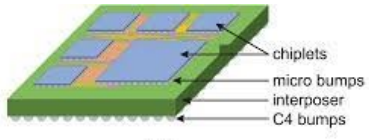
Date	1999	2005	2010	2018	2025
Technology (nm)	180	65	28	5	1
Minimum mask count	24	25	27	30	50
Wafer diameter (mm)	200	400	400	450	500
Memory samples (bits)	1G	8G	32G	10T	100T
Transistors/cm^2	6.2M	180M	330M	1.5G	20 G
Maximum number of metal layers	6-7	9	9	12	25
Clock frequency (MHz)	1250	3200	5200	20000	35000
IC sizes (mm^2)	400	596	699	750	1200
Power supply (V)	1.5-1.6	0.8-1.2	1.2-1	0.37-0.42	0.28-0.33
Number of pins	700	1957	2734	3350	4200
Number of pins	700	1957	2734	3350	4200

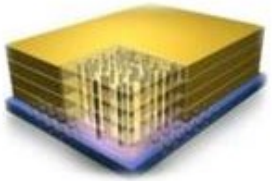
IC Design – PPA Analysis

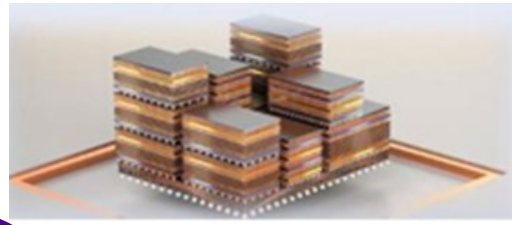


Multi-Die Systems: Types









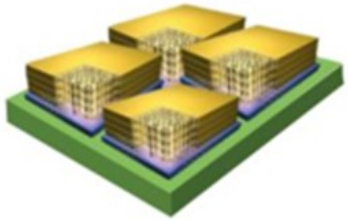
2.5D: Interposer-mounted chiplets

3D stack(s) - regular structures (memory, FPGA, …)

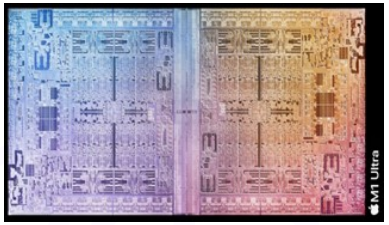
Multi-Die Systems

Recursive composition formulation … stacks of stacks

Heterogeneous stacks mounted on interposers / bridges



APPLE - M1 UltraMax CPU



2x Dies, 114B Transistors

IC Design Steps

Sign-offs

GDSII

GDSII is binary format (Not Readable)

- You can try though ….

Inverter.gds

```
02000200 60000201 1C000300 02000600 ..........`.... 000000
01000E00 02000200 60002500 01000E00 .....%.`........ 000010
42494C45 4C504D41 58450602 12002500 .%....EXAMPLELIB 000020
413E0503 14000300 02220600 59524152 RARY.."".....>A 000030
1C00545A 9BA02FB8 4439EFA7 C64B3789 .7K...9D./..ZT.. 00004
60000000 01000E00 02000200 60000205 ...`..........` 000050
58450606 0C001100 01000E00 02000200 .............EX 000060
0100020D 06000008 04000045 4C504D41 AMPLE..... 000070
```

Design description

Logic Synthesis

Floorplanning

Placement

Clock Tree Synthesis

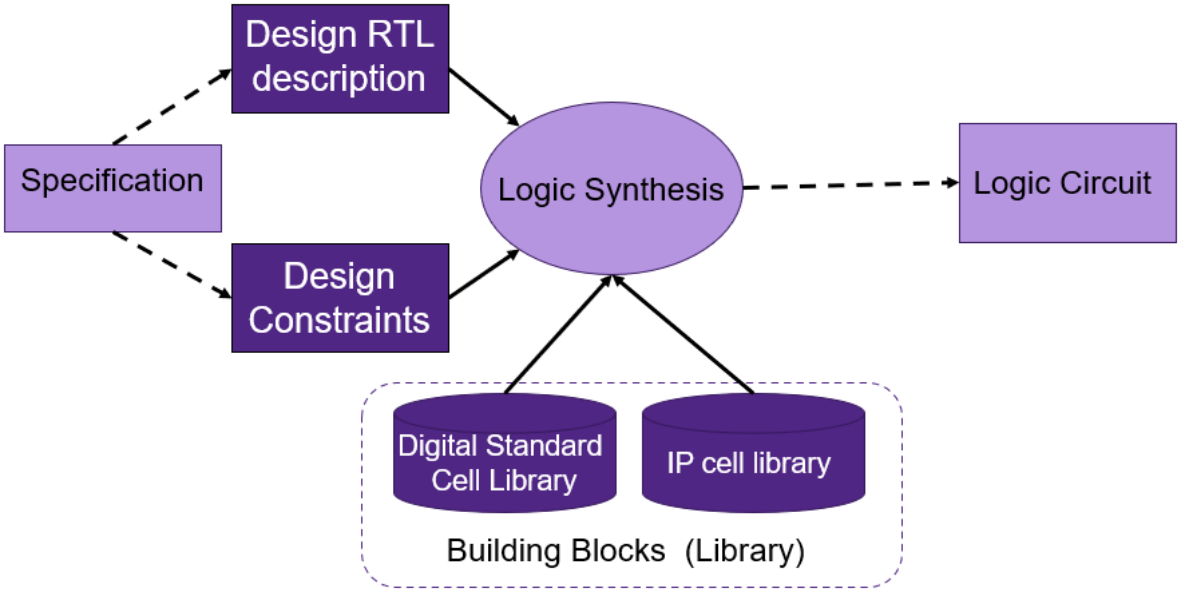
Routing

Post-Routed Layout

IC Design Steps: Logic Synthesis

Logical Synthesis

- Logical synthesis takes the RTL (register transfer level) description of a design and produces a gate-level netlist.
- Logical synthesis operates at a high level of abstraction, where it is concerned with the logical functionality of the design.



IC Design Steps: Logic Synthesis

HDL (Verilog)

- General definition

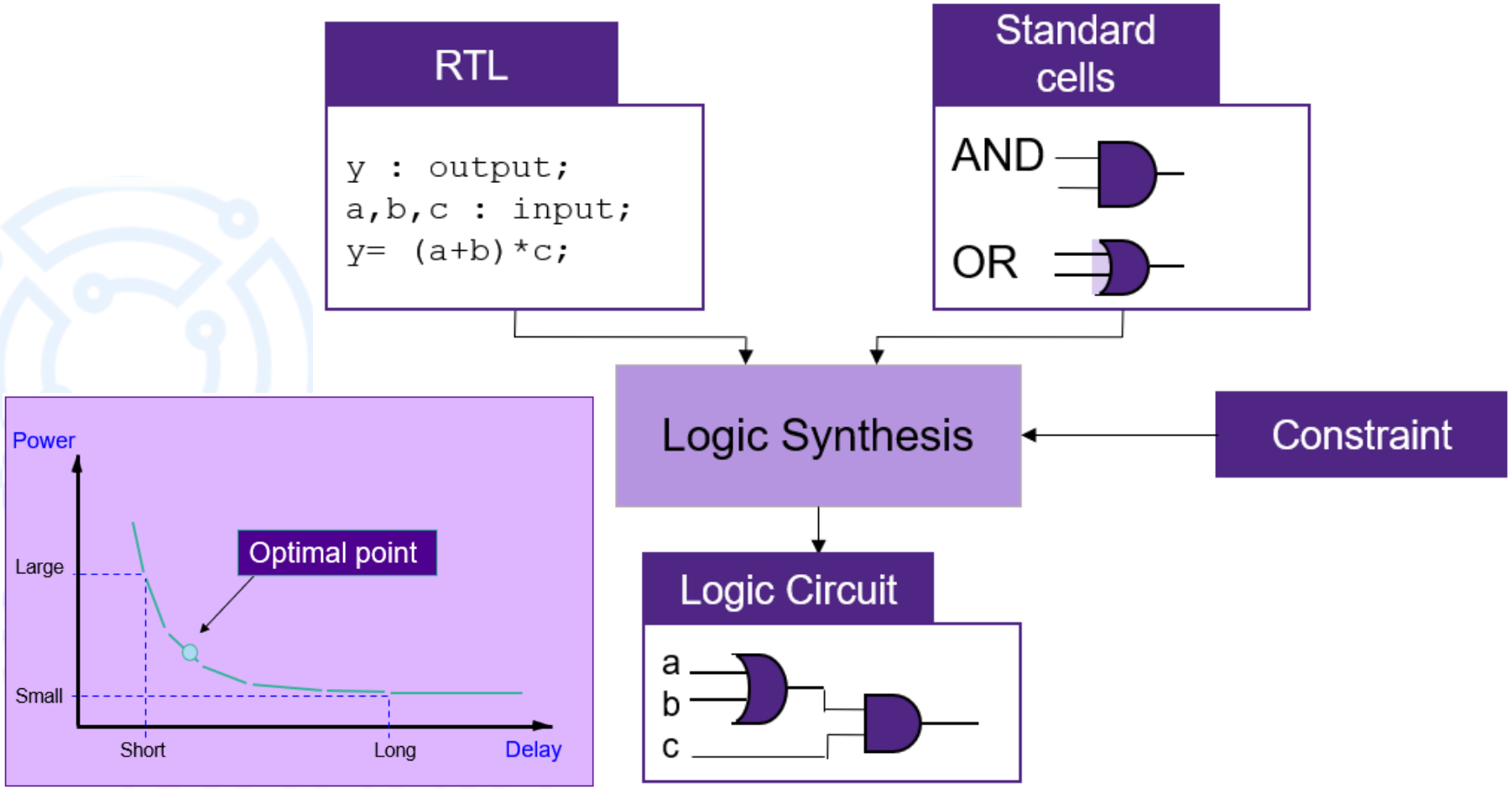
```
module module_name ( port_list );
    port declarations;
    …
    variable declaration;
    …
    description of behavior
endmodule
```

- Example

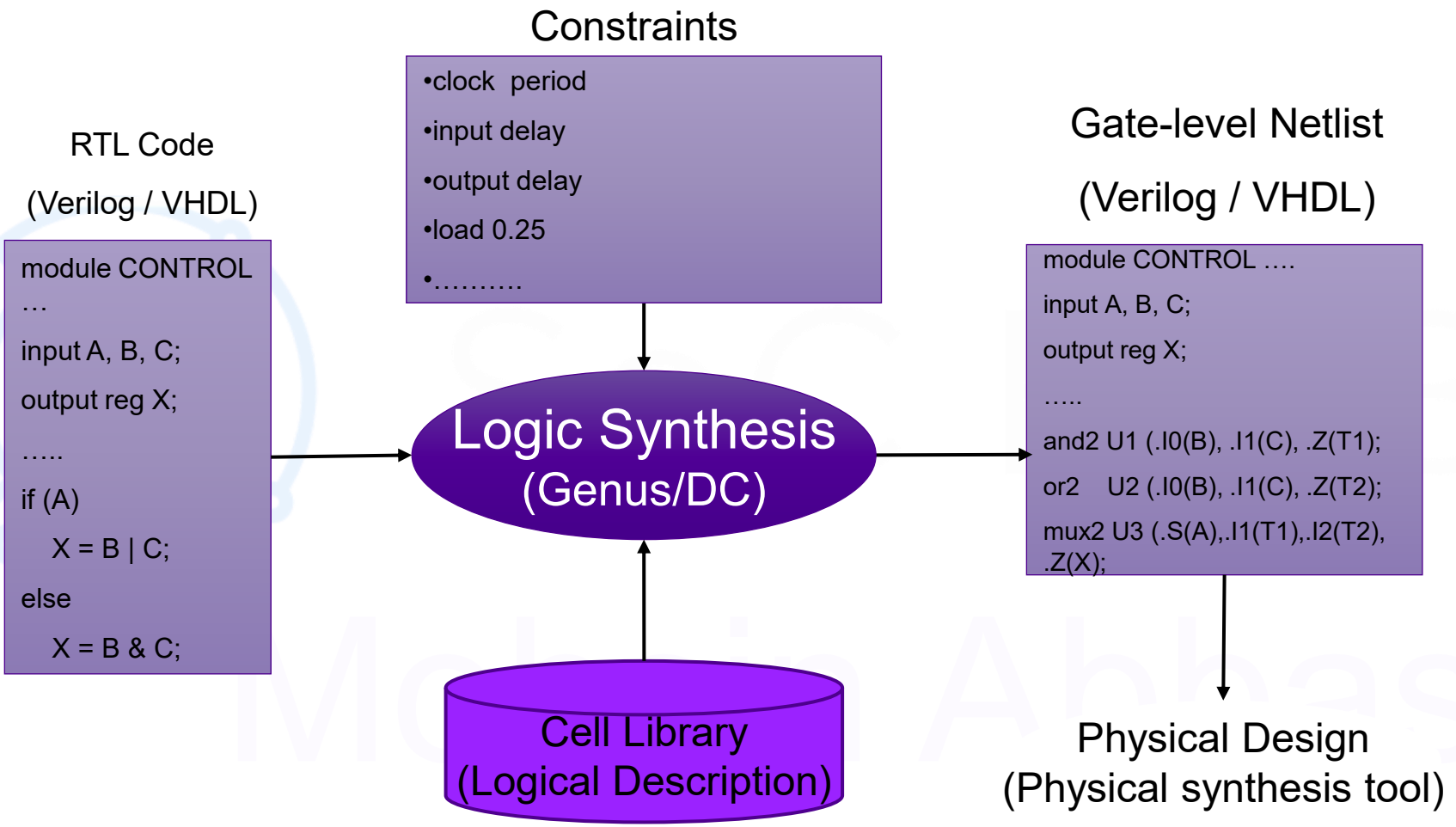
```
module half_adder(a, b, sum, carry);
    input a, b;
    output sum, carry;

    assign sum = a ^ b;  // ^ denotes XOR
    assign carry = a & b; // & denotes AND
endmodule
```

IC Design Steps: Logic Synthesis



IC Design Steps: Floorplanning

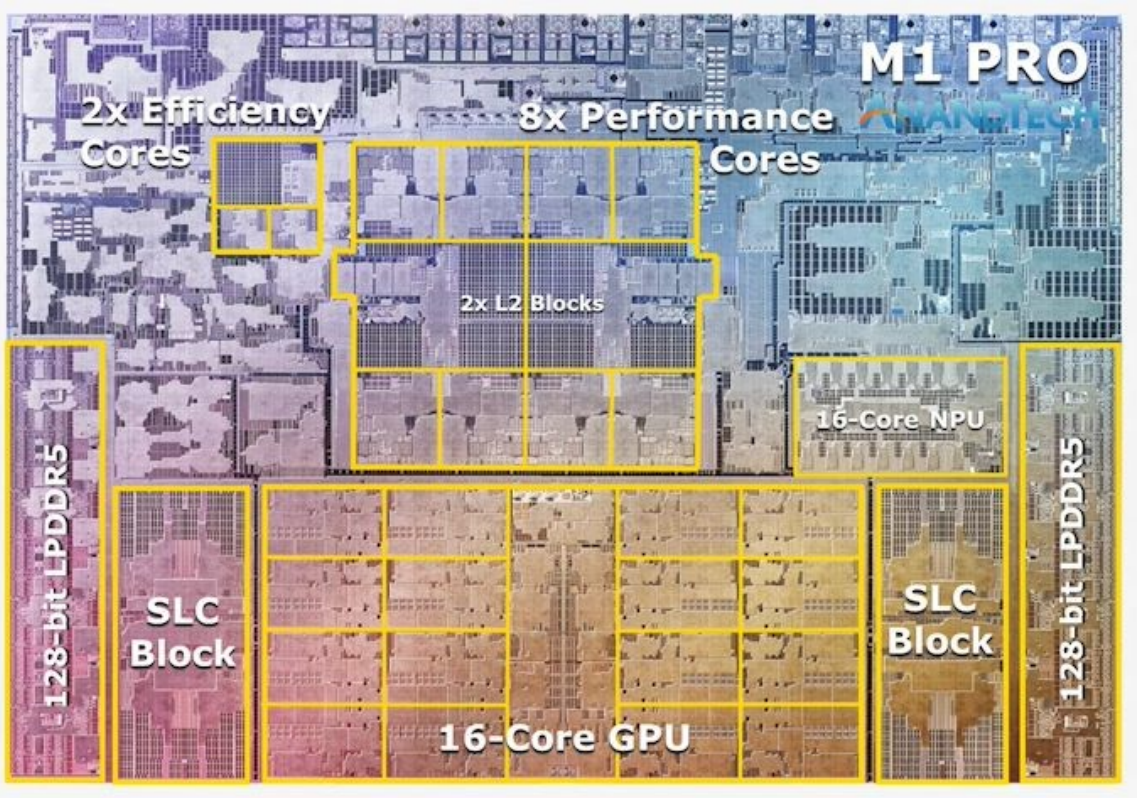


IC Design Steps: Floorplanning

- Floorplanning is a critical phase in ASIC design, where the layout and organization of various components — such as I/O pads, macros, and power/ground structures — are defined on the chip.
  - It sets the stage for subsequent design steps, including placement, routing, and timing closure.

Apple M1 : Floorplan

Basically a good floorplan will give a better Power Performance Area (PPA).



Reference. Vazgen Melikyan, Synopsys University Courseware (Synopsys confidential information)
https://www.anandtech.com/show/17019/apple-announced-m1-pro-m1-max-giant-new-socs-with-allout-performance

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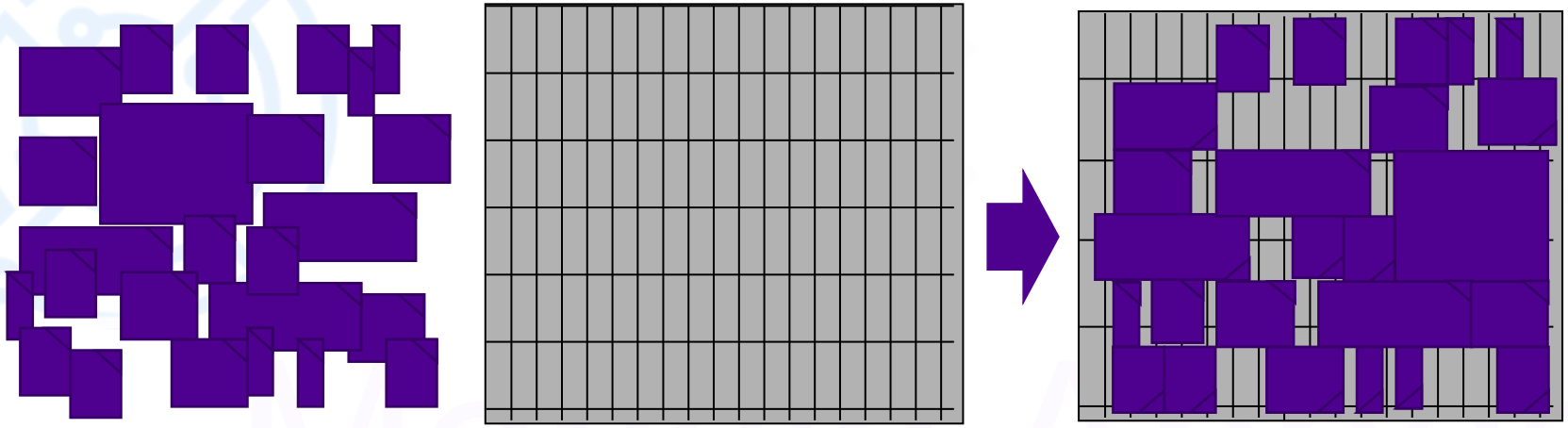
IC Design Steps: Placement

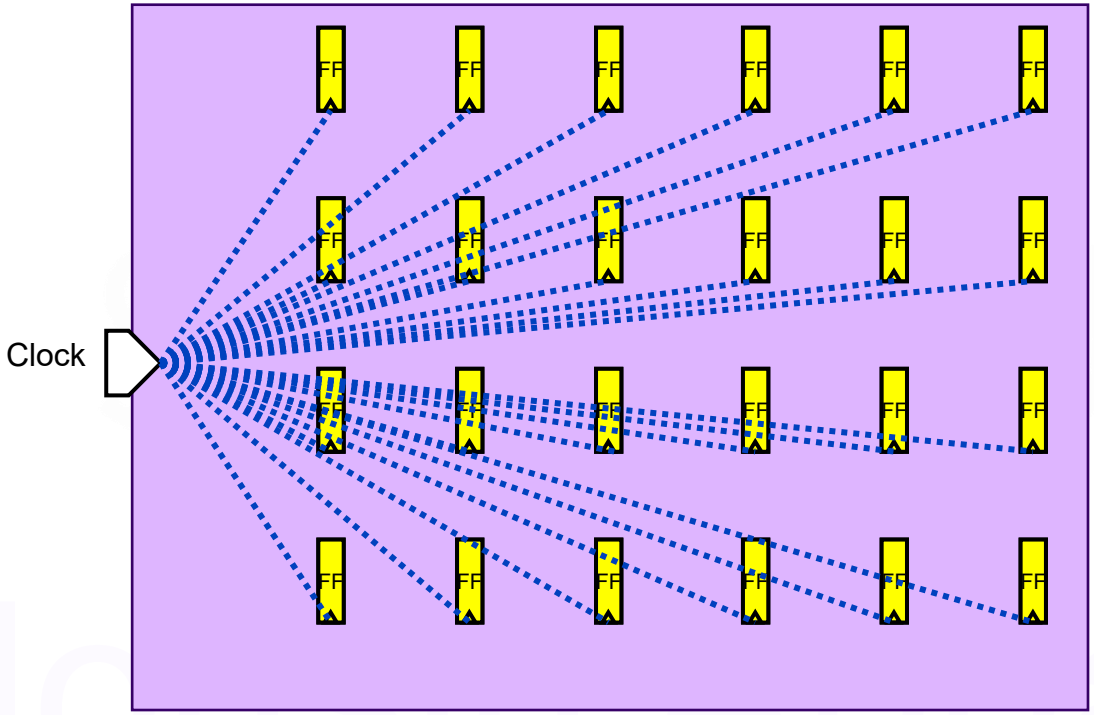
Placement is the stage where the Standard Cells are placed in the design.

- Previously in the floorplan stage **Macro** placement is done.
- Placement does not just place the standard cell available in the synthesized netlist, it also optimizes the design.



IC Design Steps: Clock Tree Synthesis

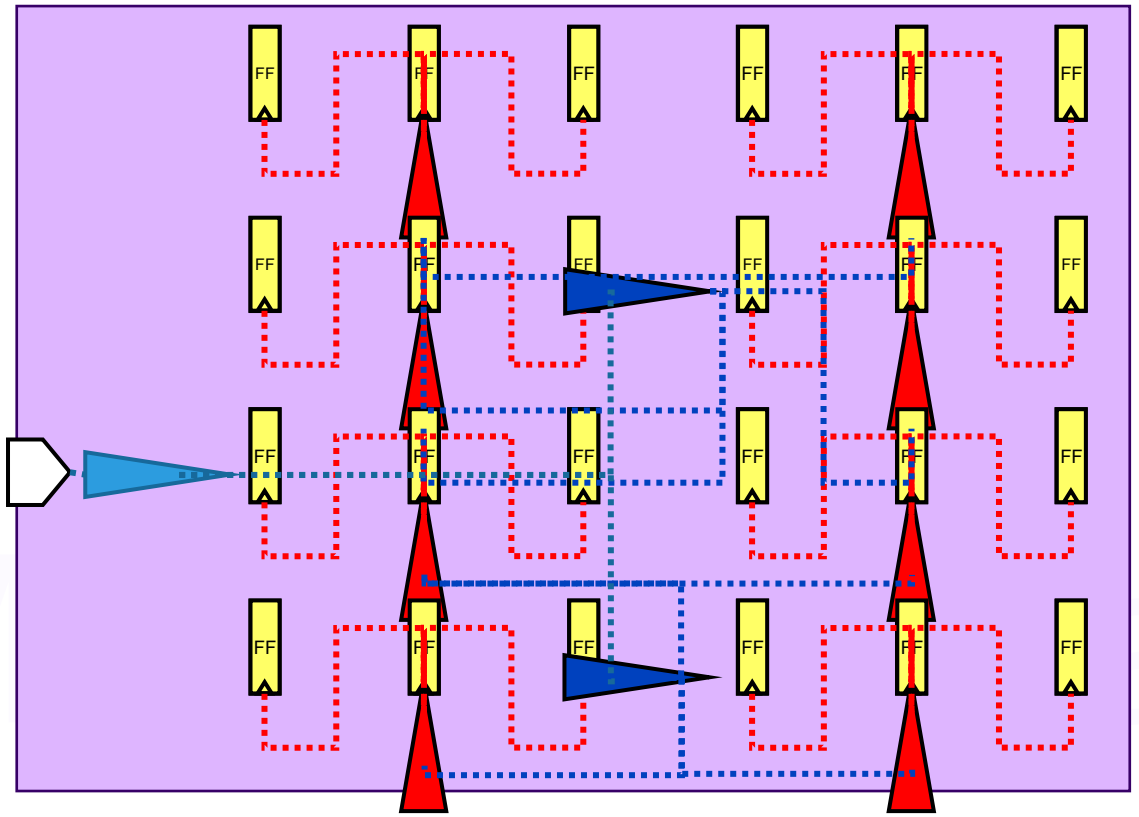
- All clock pins are driven by a single clock source



Problems ?

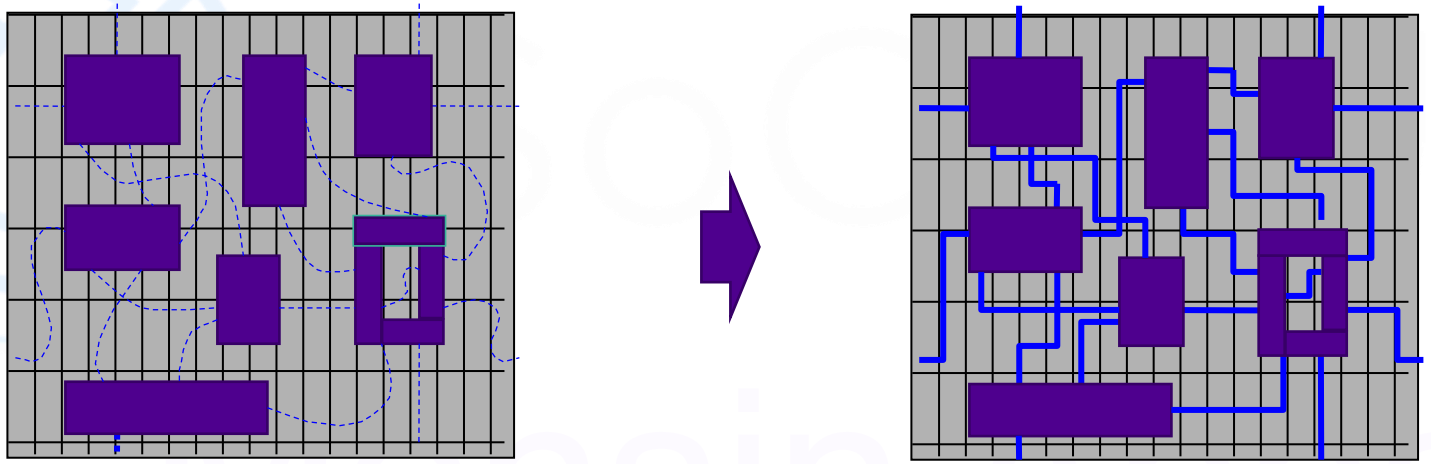
IC Design Steps: Clock Tree Synthesis

- A buffer tree is built to balance the loads and minimize the delays



IC Design Steps: Routing

- Routing is the stage after **Clock Tree Synthesis** and optimization
  - Exact paths for the interconnection of standard cells, Macros, clock and signal (I/O) pins are generated.
  - Electrical (physical) connections using metal interconnects (and vias) are created in the layout

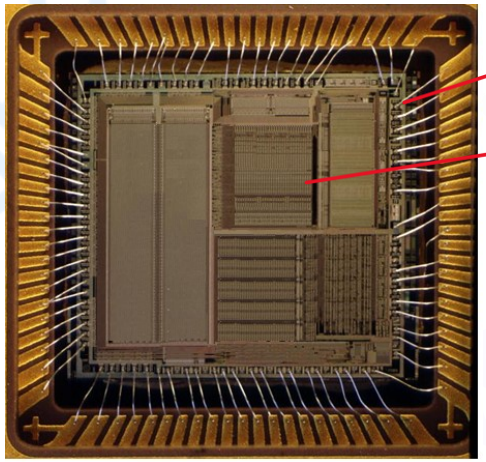


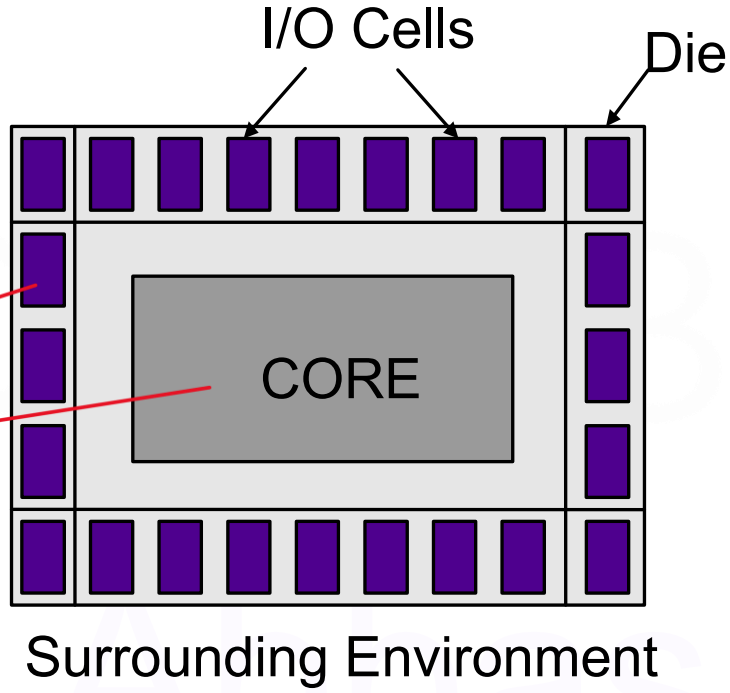
Placed design

Routed design

IC Design Steps: I/O Design

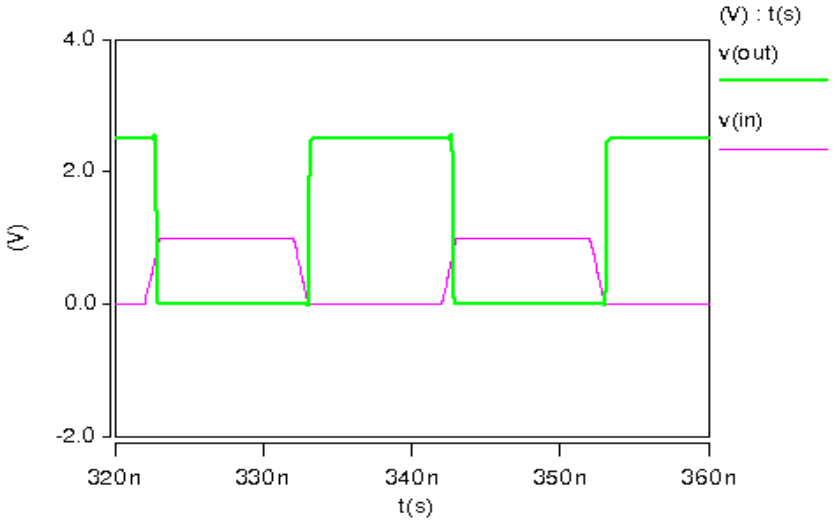
- Core - provides basic functionality of IC
- I/O Cell – provides interface between the Core and surrounding environment (voltage levels, signal transfer velocity, resistances, etc.)





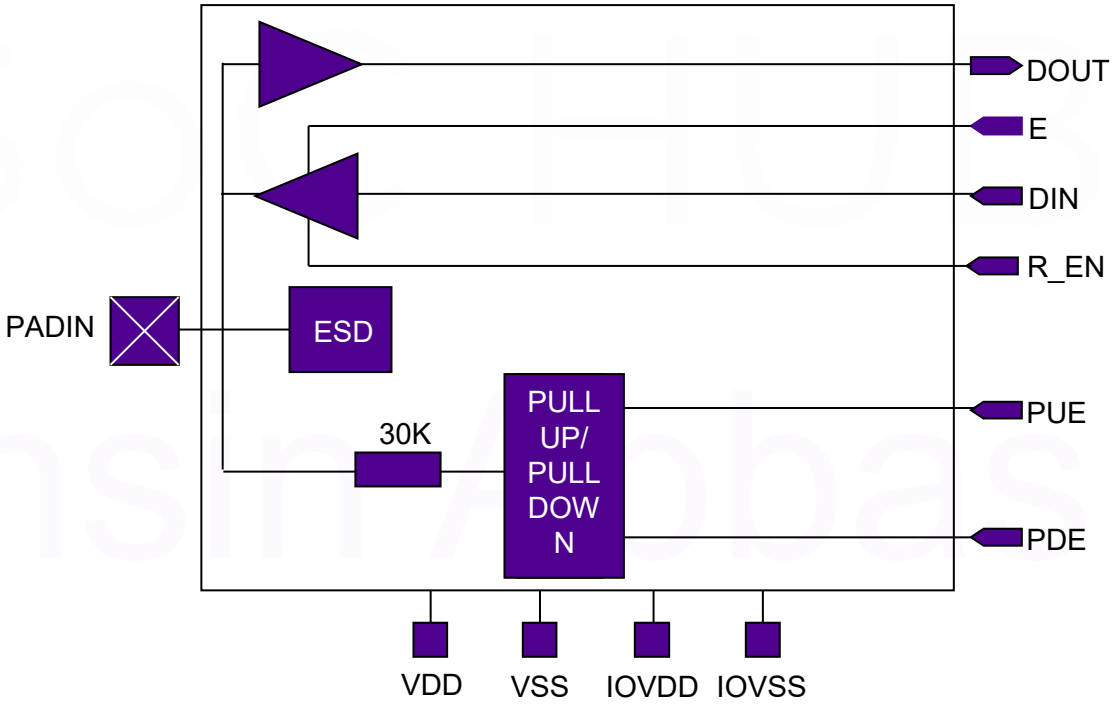
IC Design Steps: I/O Design

VDD=1.0V – to - VDDIO=2.5V



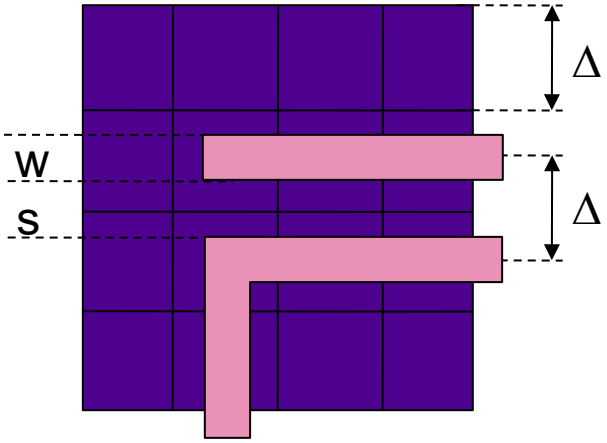
ESD protection

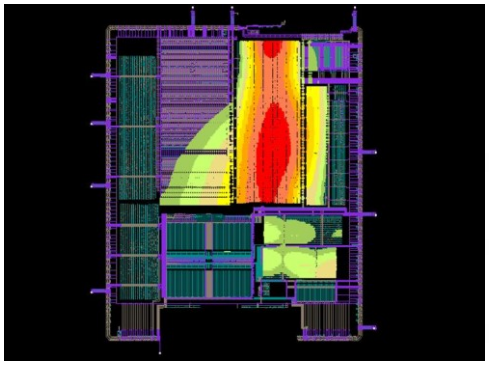
- IC is very sensitive to electrostatic discharge, I/O cell should protect IC from ESD.
- IC is subject to ESD during fabrication, packaging and exploitation processes.

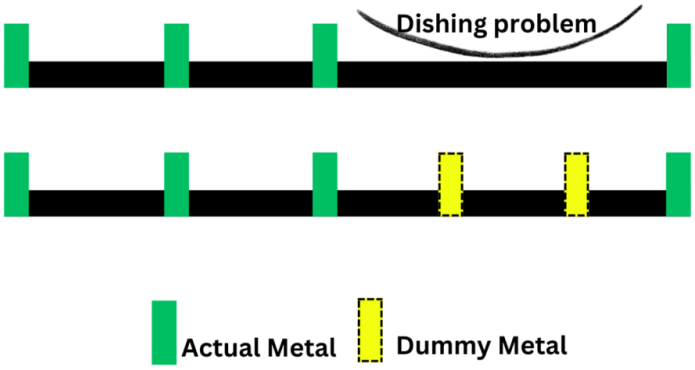


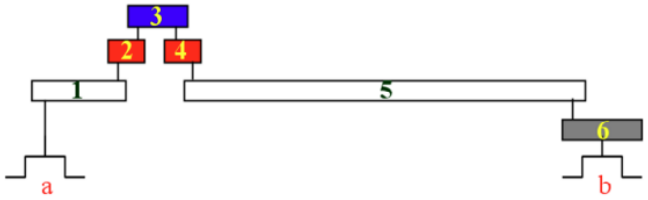
IC Design Steps: Sign-Off

- Sign-Off is the process of logical and physical verification of the chip/IC.
  - Logical
    - Logic Equivalence Checks
    - Post-layout STA
  - Physical
    - Layout Vs Schematic (LVS)
    - Design Rule Checks (DRCs)
    - Electric Rule Checks (ERC)
    - Antenna Checks
  - Power
    - Electro-Migration (EM)
    - IR Drop





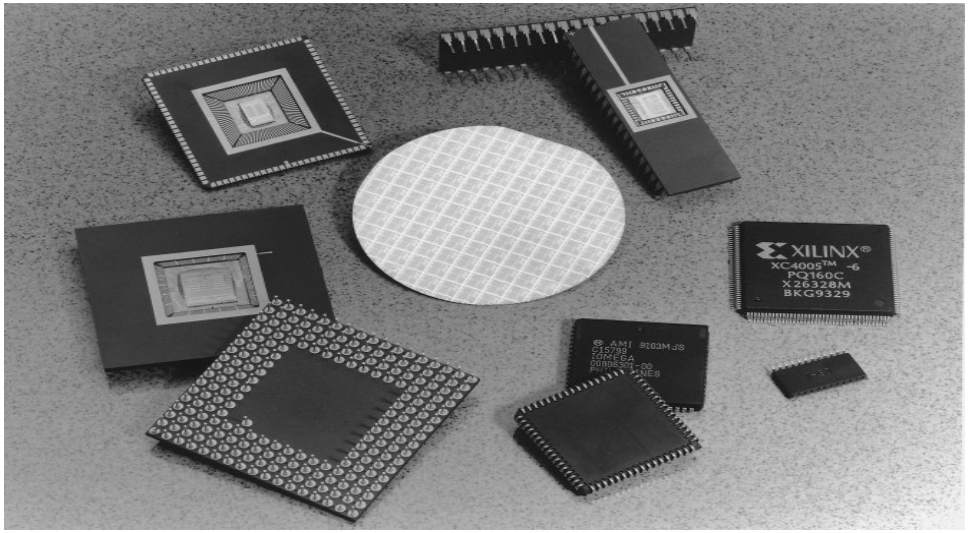


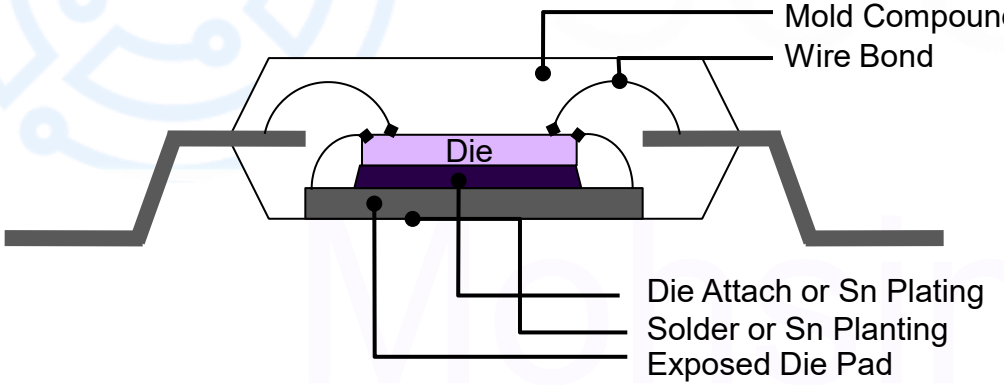


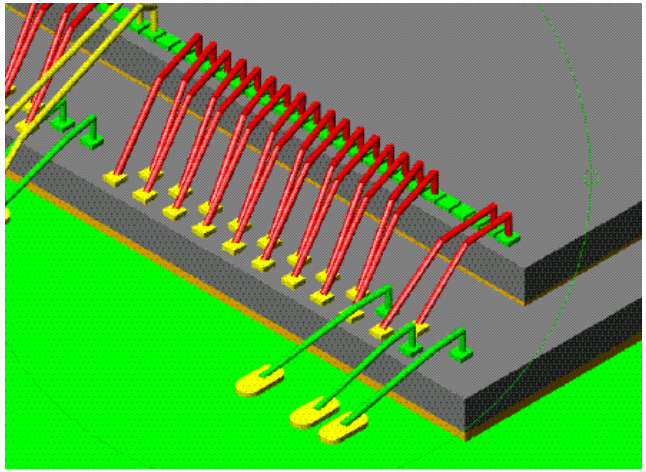
Metal 3
Metal 2
Metal 1
Poly

IC Design Steps: IC Packaging

- Package is IC holder. It provides the physical, temperature and electrical protection.







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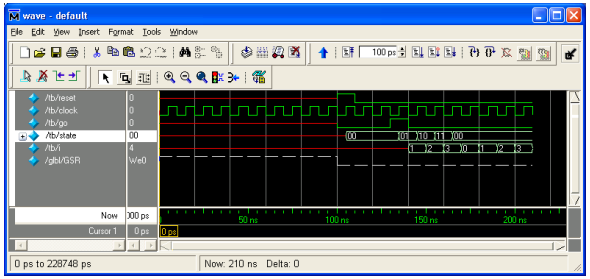
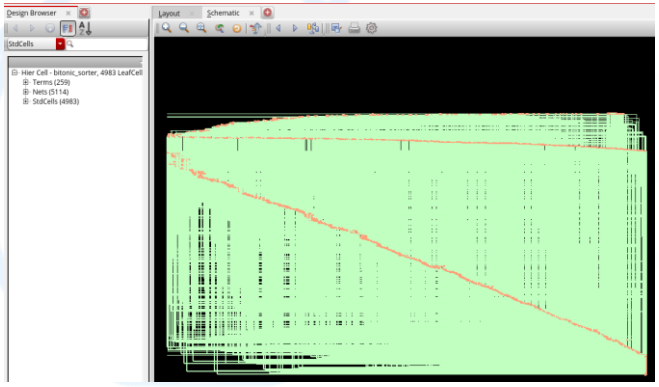
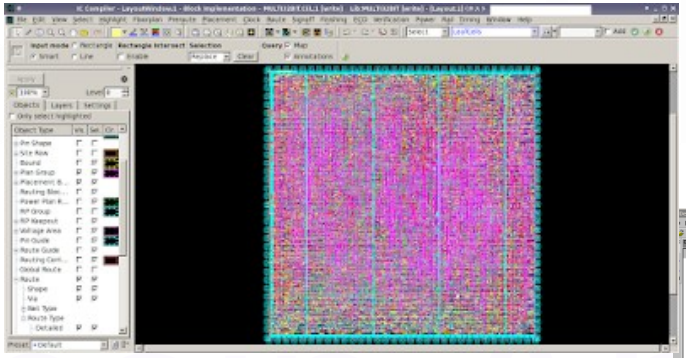
Electronic Design Automation (EDA) Tools

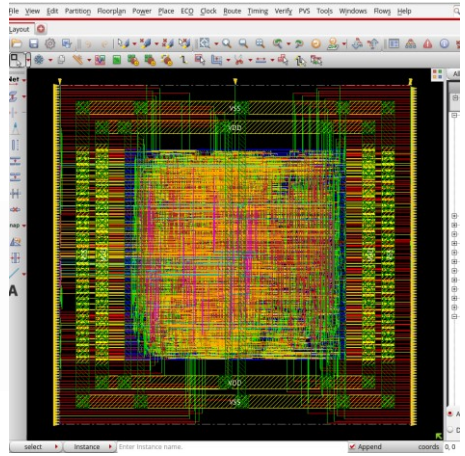
- Behavioural simulation
  - ModelSim, QuestaSim, Xcelium

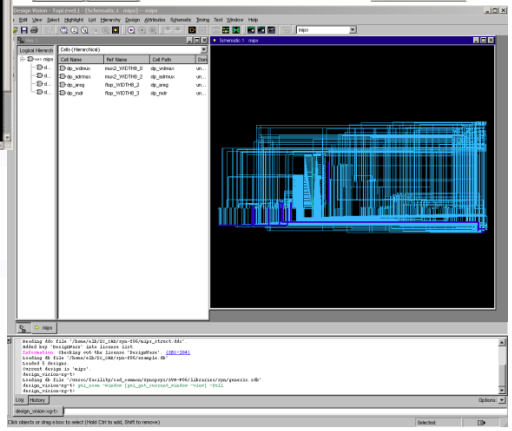


- Logical Synthesis
  - Cadence Genus, Synopsys Design Compiler









- Physical synthesis (floorplanning/placement…../GDSII)
  - Cadence Encounter/Innovus, Synopsys IC Compiler
  - Signoff tools, Tempus/PrimeTime

Reference. Vazgen Melikyan, Synopsys University Courseware (Synopsys confidential information)
https://my.ece.utah.edu/~kstevens/5710/dc-soc.pdf
https://web.mit.edu/6.111/www/labkit/simulation.shtml

Thanks

Next Lecture: RTL-to-GDSII The Bare Minimum